PHYSICAL MODELING OF THE POWER VDMOST FOR INTEGRATED CIRCUIT COMPUTER-AIDED DESIGN

By

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Abstract of Dissertation Presented to the Graduate School
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Major Department: Electrical Engineering

This dissertation presents a methodology for physical modeling of vertical double-diffused MOS transistor (VDMOST) for integrated circuit computer design. By comprising the regional models, a physical circuit model for the power VDMOST is obtained that accounts for the unique behavior of the power device. The unique features of the VDMOST such as quasi-saturation, the nonlinear interelectrode capacitances, and the reverse-recovery current are precisely modeled based on the two-dimensional as well as the three-dimensional device simulations. The composite model is implemented in Saber and SPICE2G6 code. Our new model is verified against steady-state and capacitance-voltage measurements on test devices, and against numerical simulations. A parameter extraction routine is developed and a system that links ICCAP and Saber is set up that does the measurement, the simulation and the parameter extraction. Further circuit simulation of high-voltage ICs are done utilizing the Saber model template to demonstrate the excellent performance of our model for the applications.

CHAPTER 1
INTRODUCTION

Power MOSFETs are very important devices in power circuit applications such as motor control, switch mode power supplies, and telecommunication electronics. They are unipolar devices which supercede bipolar devices for some applications. First, they have a high input resistance which ensures no significant steady-state gate current flow in either the on-state or the off-state. This simplifies the gate drive circuitry and reduces the cost of the power electronics. Then, the on-state current conduction of MOSFETs are through transport of majority carriers without the presence of minority carriers. Thus, little switching delay occurs because of the charge storage and the recombination of minority carriers during transient turn-on and turn-off as in bipolar devices. This property allows the high frequency application of the devices. Also, power MOSFETs display a good safe-operating-area characteristic, which means they endure high current and voltage (for a short duration) without undergoing destructive breakdown (second breakdown for bipolar devices) and self-heating effect.

The main drawbacks for the power MOSFETs are the higher on-resistance and the lower current handling ability when compared with bipolar devices. Even after the development of the IGBT (Insulated Gate Bipolar Transistor) which shows good on-resistance and better current handling ability, power

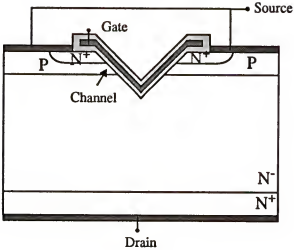
MOSFETs are still important for circuits operating at higher frequencies and at lower voltage (under 600V).

MOSFETs for power applications cannot be fabricated by merely scaling up low-power MOSFETs to the desired voltage and current. The high voltage blocking ability requires a large depletion area for the reverse-biased p-n (body/ drift) junction. Thus, the power MOSFET is evolved which contains a low-doped epi-layer that support the blocking voltage.

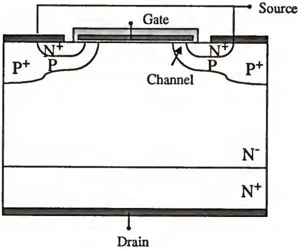
The first commercially available power MOSFET was the vertical MOSFET with V-groove technology (Fig. 1.1(a)). The V-shaped groove is formed by using an anisotropic etching to create the structure. Then, the gate oxide is grown in them. The nonplanar structure complicates the metal routing procedure. Also, the etching process is hard to control. Planar devices are preferred for both the discrete and the integrated devices.

A development that was of great importance in the power MOSFET is the utilization of double-diffused technique. The double-diffused MOSFET(DMOSFET), shown in Fig 1.1(b), is fabricated by using planar diffusion technology with a refractory gate such as polysilicon. In these devices, the body region and the source region are diffused through a common window defined by the edge of the polysilicon gate. The body region is driven in deeper than the source. The difference in the lateral diffusion between the body and the source region defines the surface channel region.

There are two categories of DMOSFETs depending on the position of the drain. The lateral DMOST (LDMOST) has the drain high-doped drain region at



(a)



(b)

Figure 1.1. Vertical MOSFETs: (a) V-shaped groove cell structure; and (b) planar DMOST cell structure.

the surface of the device. Thus, the current travels laterally between the source and the drain. The vertical DMOST (VDMOST) has an buried layer that collects the current in the epi region, so the current flows vertically in the epi region. Devices for high voltage normally require thick epi layer. The economic design of the epi thickness in junction isolated IC is 25μm, which gives approximately 250V breakdown voltage[LUD91]. Higher voltage DMOST devices are made using the lateral technology. However, the VDMOST has a better on-resistance-area product over LDMOST [WRA85][STO88], since the drain contact is not at the surface area except at the periphery of the transistor.

The monolithic integration of power DMOSFETs and bipolar or MOS VLSI circuitry, the so-called Smart Power or Intelligent Power Device (IPD) technology, has become increasingly widespread over the last 15 years. This technology combines the power handling capability with on-chip regulation of overcurrent, overvoltage, and overtemperature conditions [BAL91], as well as analog and digital functionality.

CAD simulation tools should be developed along with the matured process technology of the power devices to support optimal device and circuit design. A promising circuit model for a power device has to account for its unique physical characteristics, and yet has to be incorporated in circuit simulators with the inclusion of physical and extractable model input parameters. Most commonly used VDMOST models are a generic SPICE model within a subcircuit of additional passive elements [SIM89][Xu88][COR89]. They fail to predict the unique device characteristics such as quasi-saturation from space-charge-limited current flow and the reverse-recovery for the VDMOST. The unique device characteristics proposed by NIST (National Institute of Science & Technology, USA) for the VDMOST include 1) a nonlinear gate-drain capacitance; 2) a nonlinear gate-source capacitance; 3) a nonlinear drain/source capacitance; 4) device charge conservation; 5) body diode reverse recovery; 6) mobility variation in the channel; 7) channel length modulation; 8) a parasitic JFET; 9) a parasitic BJT; 10) subthreshold current; and 11) avalanche breakdown [NIS94].

Several physical VDMOST models for the VDMOST has been attempted to model its unique behavior. Among them, the one by Scott and Franz [SCO90] focuses on the three interelectrode capacitances, but it lacks a physical steady-state model which is the basis of accurate transient simulations. Kim and Fossum's work [KIM90] accounts for the space-charge-limited current flow which leads to the quasi-saturation effect, but it has input parameters based on a 2-D structure. Also, it lacks subthreshold characteristics, reverse-recovery characteristics, and a good model for the gate capacitance.

The focus of this dissertation is on the planar n-channel VDMOST. The purpose is to develop and implement physical models of the VDMOST for power IC CAD. The unique behavior of the nonlinear capacitances, the reverse-recovery, and the quasi-saturation effect are accurately modeled. The model is implemented in the circuit simulators Saber and SPICE2G6. The major contributions in this dissertation are

(1) the development of a systematic approach for modeling power semiconductor devices.

(2) the study of the carrier transport in the VDMOST via intensive two-dimensional and three-dimensional device simulations.

(3) the formulation and solution of the steady-state and the transient carrier transport equations for the VDMOST.

(4) the implementation of the model into Saber and SPICE2G6.

(5) the development of an ICCAP/Saber system that does the VDMOST measurement, the simulation, and the parameter extraction.

In Chapter 2, the basic semiconductor equations, namely the Poisson's equation, the continuity equations, and the current equations are reviewed. Also, a modular concept for a systematic approach of modeling power devices is developed. The basic idea is to construct a device model with basic regional models. The five basic regions, i.e., the neutral-ohmic region, the space-charge region, the MOS channel region, the high-injection region, and the current-induced space-charge region and the unified method of recognizing them via numerical device simulations are described. The method is then applied to the VDMOST to determine the basic regions for the development of a physical circuit model.

In Chapter 3, the detailed regional model equations for the VDMOST are described. The model accounts for the velocity saturation at both the source end and the drain end of the channel depending on the channel doping gradient and the quasi-saturation effect induced by the space-charge-limited current in the drift region between the P-wells. The nonlinear gate capacitance accounts for all the regions under the gate in the source/gate overlap area, the channel area, and also the surface of the drift region. A more precise modeling of the drift region driven by the three-dimensional device simulation is described, too. Also, the transient reverse-recovery current induced by the non-quasi-static effect of the parasitic PIN diode is also incorporated in the model. The equations for the temperature-dependence physical parameters, important for the power devices, are used in the model.

In Chapter 4, the VDMOST model implementation, parameters extraction, and the model validation are described. The model is implemented into Saber and SPICE2G6 codes. A parameter extraction routine is developed for the model. A system which links ICCAP with Saber and measurement equipments is constructed, so that the device measurement, simulation and parameter extractions can be manipulated by ICCAP. Measurements and the simulation result support the steady-state as well as the capacitance-voltage characteristics of the model. The model is further verified with a reverse-recovery test circuit, an inductive-resistive load circuit, a gate charging circuit, and a soft-switching circuit as examples for the model applications.

In Chapter 5, the main accomplishments of this dissertation are summarized, and suggestions for further research of the VDMOST are discussed.

Appendix A describes a behavior modeling of the VDMOST. Based on the result of the physical model simulation, a pure empirical method is proposed which is intended for a faster circuit simulation. The simulation of the steady-state characteristics for the behavior model is proven to be 5.5 times faster than the physical model.

Appendix B lists the MAST source code of the VDMOST Saber model developed in Chapter 3.

CHAPTER 2
OVERVIEW OF MODELING CONCEPT AND VDMOST OPERATIONS

Physical circuit models for semiconductor devices are derived analytically from basic semiconductor equations via a regional approach. The basic semiconductor equations are five partial differential equations, namely Poisson's equation, electron and hole continuity equations, electron and hole current equations, as will be described in the following section. By lumping the carrier transport equations and making assumptions, analytical solutions can be obtained inside basic semiconductor regions. The device model is obtained by linking the regional models with Kirchhoff laws. Usually, numerical device simulations are done first to investigate the inside carrier transport in the device. It serves three objectives: to identify the basic regions or "building blocks"; to document the unique behavior of the device; and to be used as basis for making assumptions and approximations.

The numerical device simulators used in this work are TMA PISCES (MEDICI) for two-dimensional structural simulations and TMA DAVINCI for three-dimensional structural simulations. The input requirement for the device simulators are the device structure and the operating conditions. The device structure includes layout information, doping profile, and terminal positions. The operating conditions are the applied voltages or currents within the interested operating regions.

In the first section, the basic equations used to describe semiconductor devices are reviewed. In Section 2.2, the concept of physical regional modular models including the definition of the basic regions and the equations to be solved for the regions are presented. Then, the VDMOST structure is described and the structure for numerical device simulation is constructed. Section 2.4 depicts the VDMOST operation and characteristics by PISCES simulations. The regional partitioning of the VDMOST is concluded from the PISCES simulations in the last section.

2.1 Basic Semiconductor Equations

The electrical behavior of a semiconductor devices is governed by five basic equations, namely Poisson's equation, electron and hole continuity equations(2.1~2.3), and electron and hole current equations(2.4,2.5),

$$\varepsilon \nabla E = q\,(p - n + N_D - N_A) \tag{2.1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla J_n - U_n \tag{2.2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla J_p - U_p \tag{2.3}$$

where E is the electric field, n and p are the electron and hole concentrations, ε is the permittivity, q is the electron charge, N_D and N_A are the N and P doping concentrations, U_n and U_p are the electron and hole net recombination rates. From Boltzmann transport theory, J_n and J_p, the electron and the hole currents, can be written as functions of E, n, and p, consisting of drift and diffusion components

$$J_n = qu_nEn + qD_n\nabla n \tag{2.4}$$

$$J_p = qu_pEp - qD_p\nabla p \tag{2.5}$$

where μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the electron and hole diffusivities. There are many mobility models, such as the Arora mobility model, the carrier-carrier scattering mobility model, parallel and perpendicular field dependent mobility model, the Hewlett-Packard mobility model, etc., emphasizing different effects. The five basic equations can fully describe the conventional semiconductor devices behavior (energy balance equations are needed for small geometry devices). For the VDMOST, the field is the most important effect for the mobility. A simple field-dependent mobility is

$$\mu = \frac{\mu_0}{1 + \frac{\mu_0 E}{v_{sat}}} \tag{2.6}$$

where μ_0 is a constant low-field mobility and v_{sat} is the saturated electron or hole velocity, which are different in the regions due to different doping concentrations. A perpendicular-field-dependent mobility model must be used in MOS channel area as will be described in the next chapter.

The variables E, n, and p can be solved as a function of position (on a grid point) in the transistor using numerical device simulators. This method can be applied to all kinds of geometrical structures and different operating conditions. Theoretically, it gives precise solutions if the mobilities and the recombination rates are accurate. A serious drawback of the simulation method is that it is very CPU intensive to solve the equations simultaneously by numerical methods. Fortunately, not all three equations are important in every regions of the device. By lumping regions, making assumptions and neglecting the insignificant equations and terms, analytical solutions of the current-voltage relations might be obtained in each region. Utilizing Kirchhoff network to link the regions, the device performance is obtained which has the speed and CPU resources advantage, yet still maintain structural dependence for the model. This is often referred as physical circuit modeling.

2.2 Modular Concept

The modular concept for physical device modeling requires a well defined regions. There is some literature regarding systematic approaches for modeling power semiconductor devices [ALL94][DIE94][HOL94][MA94], [MOR94]. None of them has complete regions for semiconductor power devices. In Table 1, the five semiconductor power device regions with the region criteria and the basic equations to be solved in the region are listed.

2.2.1 Neutral-Ohmic Region

A neutral-ohmic region is defined as a region in the current path where the majority carrier concentration is approximately the background doping, and the minority carriers are negligible. For a uniformly doped region, the transport is mainly by majority carrier drift current. For a non-uniformly doped region, the diffusion transport takes part, too. The current equations in (2.4) (for N-type) and (2.5) (for P-type) are used to describe the voltage drop in this region. The diffusion terms (second terms) in (2.4) and (2.5) are neglected for uniformly doped regions.

2.2.2 Space-Charge Region

Space-charge can be induced in a P-N junction region or at the surface of MOS structure (included in field-effective region). Poisson's equation in (2.1) is used to describe the relation between the charge and the electric field in this region. To be able to obtain an analytical solution, the depletion approximation, which assumes the carriers are completely depleted, are usually used.

2.2.3 MOS channel region

MOS channel region is located at the surface of the semiconductor in MOS structures, and is easy to recognize. By varying the gate voltage, inversion, depletion and accumulation can occur in this region. By varying the drain

Table 2.1: Basic regions for power semiconductor devices

Region	Conditions	Equations
neutral-ohmic region	majority carrier is about background doping minority carrier is negligible $n = N_D$	Cur.E.
space-charge region	carrier depletion ($n = p = 0$ depletion approximation)	P. E.
MOS channel region	in MOS structure, carrier depletion, accumulation or inversion	MOS.E.
high-injection region	both carrier concentrations are higher than the background doping $n = p$	A.T.E.
current induced space-charge region	high field gradient excess majority carrier at the current path.	P.E. Cur E.

Note:
Cur.E. is the current equation in (2.4) and (2.5).
P.E. is the Poisson's equation in (2.1)
MOS.E. is the MOS current equation in (2.7)
A.T.E. is the ambipolar equation in (2.8)

voltage in strong inversion, the device can operate in the linear or the saturation region. From the MOS current equation, which is derived from the current equation, if the gate/source voltage is greater than the threshold voltage, the channel current is

$$I_{CH} = \frac{W}{2L}\frac{\mu_{eff}}{C_{OX}+C_D}\left(Q_0^2-Q_L^2\right) \tag{2.7}$$

where W and L are the width and the length of the channel, μ_{eff} is the effective channel mobility which is affected by both the transverse and longitudinal fields, C_{OX} and C_D are the oxide and channel depletion capacitances, Q_0 and Q_L are the charges at the source and the drain ends of the channel. Current saturation occurs when the carrier velocity saturates in the channel for short channel devices. The detailed calculation of the linear and saturation MOS current will be discussed in Chapter 3.

2.2.4 High-Injection Region

For power bipolar devices, the base region is low-doped and operates in high-level injection. The electron and hole concentrations are much higher than the background doping, so they can be assumed equal due to quasi-neutrality. The carriers are transported by both drift and diffusion. Recombination is important in this region. By assuming $n = p$, the electron and the hole continuity equations can be redefined as the ambipolar transport equation, which describes the excess carrier distribution in the region

$$\frac{\partial p}{\partial t} = D_a \frac{\partial^2}{\partial x^2} p - \frac{p}{\tau_a} \tag{2.8}$$

where D_a is the ambipolar diffusivity, which is $2D_n D_p / (D_n + D_p)$ and τ_a is the high-injection carrier lifetime. Knowing the carrier distribution, the current density can be described by (2.4) or (2.5). The stored charge in the region is also known.

2.2.5 Current-Induced Space-Charge Region

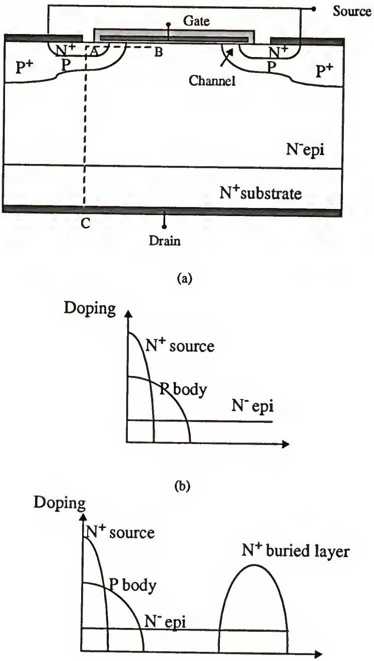
The current-induced space-charge is not uncommon in power devices because high currents in the low-doped regions result in a high electric field. Once the field reaches its critical value, the carrier velocity saturates, and excess carriers are generated in the region. The current-induced space-charge causes a higher voltage drop compared with the ohmic voltage drop across the region which can be described in the Poisson's equation and the current equation. Excess carriers induced by the current and a large variation of the field are observed in this region. Both Poisson's equation and the current equation are needed to describe the region.

The solutions for carrier transport in all the regions also depend on the effective areas of the region. With the regions defined, current densities, electric fields, and charge densities can be derived to current sources, voltage drops, and total charges for the regions. These regional models can be linked to construct power device models. In order to identify the regions, the transistor device simulation must be performed to provide insight into the device behavior. By tracking down the current flowline and the carrier distributions in the device, the effective areas of all regions are defined according to the conditions listed in Table 1. To be able to obtain a analytical form for the solution, simple geometric shapes of the regions must be assumed.

2.3 VDMOST Structure

A VDMOST structure (Fig. 2.1.) [LU88] is different from a low-power MOSFET structure in the following aspects: 1) the source and drain (drift region) are not symmetric; 2) it has a long vertical, low-doped drift region, so that high-voltage application is achievable; 3) the gate is fabricated across both the channel and the drift region, so an accumulation layer is formed in the linear operating region to enhance the conductivity (the accumulation layer is replaced by depletion charge that contributes to dQ_{GD}/dt when the gate to drift region surface voltage is larger than the flat-band voltage (at high V_{DS})); 4) the source contact overlaps the p-base region to short circuit the source/body junction, so that the parasitic BJT is normally off; and 5)the channel region has a graded doping.

A more complete VDMOST device structure also includes a buried layer, a field plate, and a guarding ring as shown in Fig. 2.2. Here, the drain current is collected in a buried layer and brought up to the surface through deep N^+ dif-



(a)

(b)

(c)

Figure 2.1 The structure of a VDMOST: (a) the device cross-section; (b) the doping profile along the line AB; and (c) the doping profile along the line AC.

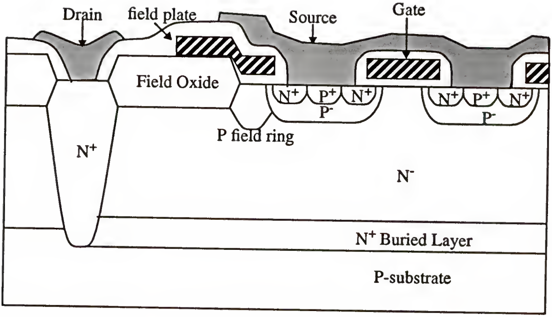


Figure 2.2 Cross-section of a VDMOST, with a buried layer and a deep N diffusion for up-drain structure. Also, a P-well field ring and a field plate at the edge of the active area are for high field protections.

fused zones. To reduce the resistance in the buried layer, the drain contact is usually designed with a fingered structure. The field plate and the floating field ring at the edge of the active area (P well region) are used to increase the breakdown voltage. It is important to know the overall device structure for physical modeling because the geometrical device parameters are used as inputs into the model herein.

The cell layout on the surface is another important issue. The VDMOST structure allows the designer to work with any conceivable cell topology as long as it meets technological constraints. Square, circular, and hexagonal cell topologies are the most commonly used window shapes (Fig. 2.3). It has been shown that the on-resistance of all cellular designs are equal if the size of the cell window and the ratio of the area of the cell window to the total cell areas are kept the same[HU84]. The three-dimensional structure will be simulated and investigated in the following chapter.

By knowing the real structure of the VDMOST, a cell structure which is the basis of a device can be constructed for the device simulator. The two-dimensional PISCES simulation input file is shown in Fig. 2.4. It specifies the grid size, the regions, the contacts, and the doping profiles of the device. The constructed structure is in Fig. 2.5.

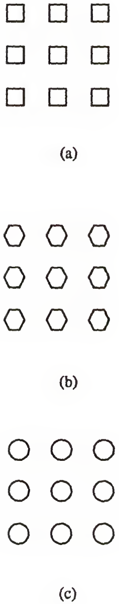


Figure 2.3 Regularly used window shapes for the VDMOST cells: (a) square; (b) hexagonal;, and (c) circular.

```
TITLE        vdmos

comment define the rectangular grid
mesh         rect nx=50 ny=50 smooth=1
x.m          n=1         l=0
x.m          n=21        l=21
x.m n=36     l=27
x.m          n=50        l=35
y.m          n=1         l=-0.1
y.m          n=2         l=0
y.m          n=28        l=10
y.m          n=42        l=38
y.m          n=50        l=42

comment eliminate mesh in drift region
eliminate    y.direc     ix.l=1 ix.h=38 iy.l=30, iy.h=40

comment      region
region       num=1 ix.l=1 ix.h=50 iy.l=1 iy.h=2 oxide
region       num=2 ix.l=1 ix.h=50 iy.l=2 iy.h=50 silicon

comment      electrode (#1 source,#2 gate,#3 drain)
electr       num=1 ix.l=1 ix.h=10 iy.l=2 iy.h=2
electr       num=2 ix.l=21 ix.h=50 iy.l=1 iy.h=1
electr       num=3 ix.l=1 ix.h=50 iy.l=50 iy.h=50

comment doping
profile n-type uniform n.peak=5e14
+            x.peak=0 width=35 y.peak=0 depth=42
profile n-type uniform n.peak=1e19
+            x.peak=0 width=35 y.peak=40 depth=42
profile p-type n.peak=1e17 x.peak=0.0 x.right=23
+     y.peak=0.0 y.junctio=5.0 xy.ratio=0.4
profile p-type n.peak=1e18 x.peak=0.0 x.right=8
+     y.peak=0.0 y.junctio=8.0 xy.ratio=0.5
profile      n-type n.peak=1.0e19 x.peak=7.5 x.right=21.5
+            y.peak=0.0 y.junctio=2 xy.ratio=0.75

comment regrid by the doping
regrid       doping log ratio=2 smooth=1 outf=vdmesh


comment Specify contact and model parameters
contact      num=2       n.poly
models       fldmob srh

comment      solve initial condition
symb         carriers=0
method       iccg damped
solve        init outf=vdouta

end
```

Figure 2.4 PISCES input file constructing the VDMOST.

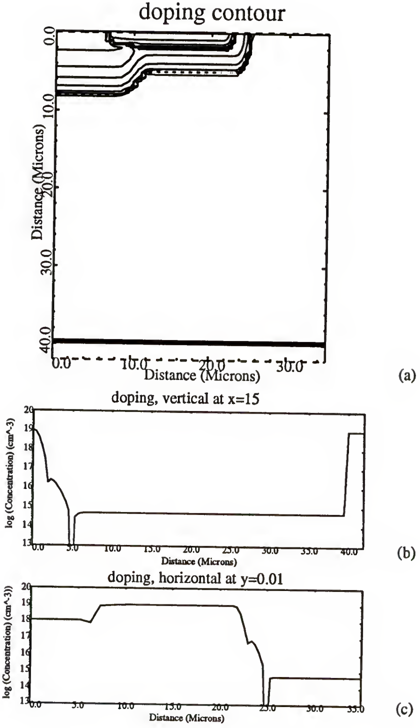


Figure 2.5 The constructed VDMOST by the input file in Fig. 2.4. with (a) the doping contour, (b) the doping profile at x=15μm, and (c) the doping profile at the surface of the semiconductor.

2.4 The Device Simulations of the VDMOST

The VDMOST can be operated in the linear, the saturation, the quasi-saturation, forward blocking and also the reverse bias regions as shown in Fig. 2.6.

Like the low-power MOSFET, the VDMOST is turned on when the gate voltage is higher than the threshold voltage forming an inversion layer under the gate as a conducting path. In forward operation, the electrons flows from the source, through the channel and the conductivity modulated accumulation layer at the surface of the epi-layer, then spreading into the epi-layer, and being collected in the buried layer that is linked to the drain contact. Figure 2.7. shows the current flowline in this condition. There is a significant ohmic voltage drop in the epi region, especially the JFET area between P-wells, as well as in the channel region as shown in the potential contour in Fig. 2.8. The electron concentration contour is in Fig. 2.9, which shows the excess electron carriers in the channel and in the drift region under the gate. Electron depletion at the p-body/ n-epi junction is also observed. These charges contribute to the transient current, so they should be modeled accurately.

As V_{DS} increases, the VDMOST enters the saturation region as the electron velocity saturates in the channel. Kim and Fossum claim that saturation occurs at the source end of the channel for graded-channel devices because the inverted electron concentration is higher at the drain end of the channel [KIM90]. However, PISCES simulation for the device reveals that the highest longitudinal fields in the channel region are close to the drain end (Fig. 2.10.). Either situation can occur depending on the channel region doping gradient and

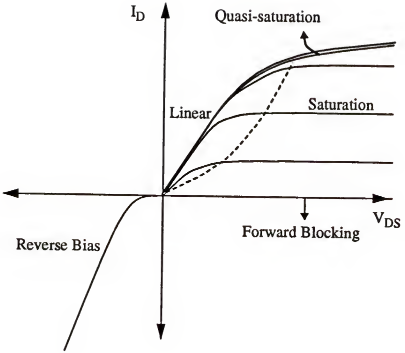


Figure 2.6 I-V plot of a VDMOST, showing linear, saturation, quasi-saturation, forward blocking and reverse bias operating regions.

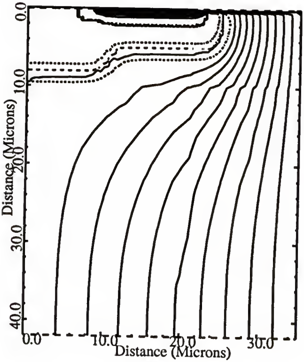


Figure 2.7. PISCES simulated current flowline in linear operating region (V_{GS}=10V, V_{DS}=5V).

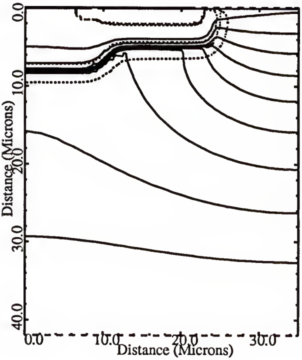
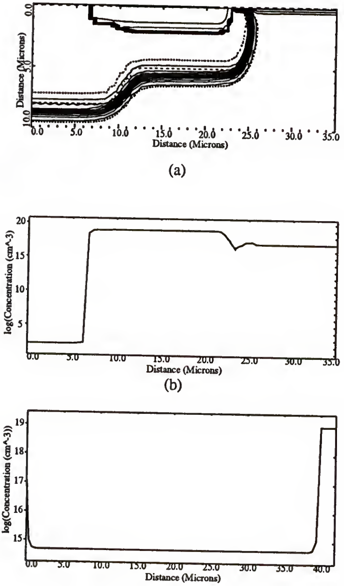


Figure 2.8. PISCES simulated electron fermi-level contour in linear operating region (V_{GS}=10V, V_{DS}=5V)



(a)

(b)

(c)

Figure 2.9. PISCES simulated electron concentration in linear operating region (V_{GS}=10V, V_{DS}=5V): (a) electron contour; (b) along the surface under the gate; and (c) along the right boundary.

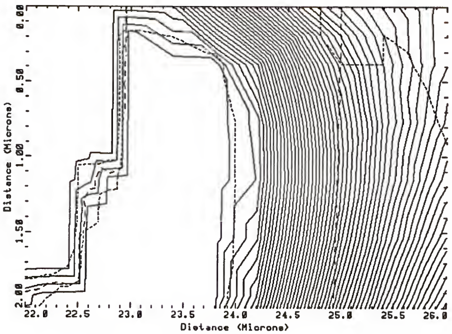


Figure 2.10. PISCES simulated potential contour in the vicinity of the VDMOST channel region (V_{DS}=50V, V_{GS}=8V, ΔV=0.2V).

the channel length. For an extreme case, if the channel is very long or the doping gradient is very small, it resembles a conventional uniform doped channel. Then the current saturates when electron velocity saturates at drain end of the channel. The other extreme case is if the gradient is very high, the inverted electron concentration is much higher at the drain end than the source end, the field will be higher at the source end and the velocity will saturate there. The next section discusses both channel models quantitatively. Unlike a conventional MOSFET, after the current saturates, a further increase in V_{DS} results in a larger voltage drop at the epi-side of the device instead of in the p-body region because the doping concentration is lower in the epi-region than in the p-body region.

The high-voltage VDMOS transistor exhibits a limitation in the current level, i.e., quasi-saturation. It is shown that such behavior is due to carrier velocity saturation in the JFET formed between the p-body wells in the drift region under the gate of the device [DAR86]. When the field exceeds the critical field, the carrier velocity saturates. A further increase in the current depends on the increase in carrier concentration. Thus, a current-induced-space-charge layer is formed, which causes a large voltage drop across the region, and limits the current. The current increase very little with V_{GS} in quasi-saturation. This phenomenon can be seen by the current equation with the effective field mobility model

$$I_D = A_y q n \frac{\mu_{nd} E_y}{1 + \frac{E_y}{E_c}} \tag{2.9}$$

where A_y and E_y are the cross-sectional area and the electric field at the position y, respectively, n is the electron concentration, μ_{nd} is the low-field mobility, $E_c = v_{sat}/\mu_{nd}$, is the critical field when the electron velocity saturates. Further increase in V_{DS} cause the electron concentration in the JFET region to increase but the current I_{DS} increases at a much lower rate than in the linear region. The relation between the field and the carrier concentration can be determined by the Poisson's equation neglecting the hole terms

$$\varepsilon_s \frac{dE_y}{dy} = q(n - N_D) \tag{2.10}$$

Figure 2.11 shows PISCES simulations of the electron concentration and the field in the epi-region along x=35µm line in quasi-saturation operation. Excess electron carriers induced by the current and a high field gradient are observed in the JFET region. Note there is a dipole layer where the electron concentration is slightly lower than the background doping with the decrease of the field as defined by Poisson's equation.

The device can also be operated in the reverse mode (V_{DS}<0) as a PIN diode formed by the p-body, n-epi, and N^+ drain regions. The diode has a long reverse-recovery time due to the low doping in the N-epi region. By switching the device on and off in the reverse mode, the device can be used to replace the

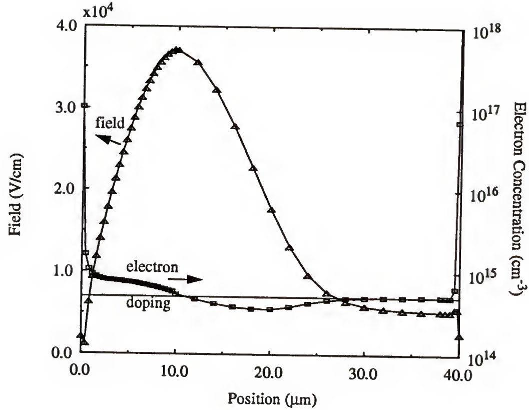


Figure 2.11 PISCES simulated field and electron concentration in the drift region (V_{GS}=12, V_{DS}=50, along x=35μm line).

Schottky diodes in dc-dc converter applications [LIA93]. Figure 2.12 shows the current flowlines in reverse operation. Note that in this operating region, the P-body/N-epi junction is forward-biased and the device functions as a diode. Figure 2.13 shows the carrier and the doping concentrations as a function of the vertical directions at x=0 and V_{DS}=-1V. The carrier distribution shows the turn-on of a PIN diode with high injection in the low-doped N-epi region.

When the device is Off, all of the drain/source voltage drops across the P-body/N-epi junction. Figure 2.14 shows the potential distribution of the device when the gate is shorted to the source and the drain voltage is 25 volts with respect to the source. The depletions regions are mostly in the low-doped N-epi region. Note that the N-epi region under the gate is also depleted because of the potential difference between the gate and the drain. The blocking capability for the power MOSFET is of great interest for the device applications. The cell breakdown voltage depends on the epi doping and the depth of the same region for Avalanche breakdown. Punchthrough might occur before the Avalanche breakdown when the breakdown is caused by the body/epi depletion region reaching through the p-body region and is never the intention for the device design.

A parasitic N^+-P-N vertical bipolar structure can be found in the VDMOST. Due to the existence of the p-body pinch resistance, a voltage drop can occur across the p-body/source junction if there is a large current flow in the pinched-p-body region. The forward-biased P-body/N-source junction turns on the down-mode BJT (with $N^+/P/N^-$ as emitter/base/collector). The current comes

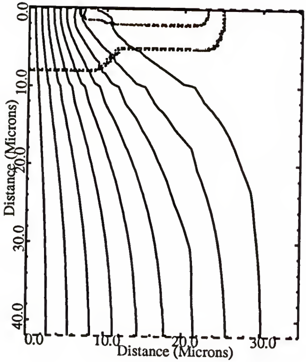


Figure 2.12 PISCES simulated current flowline in the VDMOST in the reverse operating region (V_{DS}=-1V).

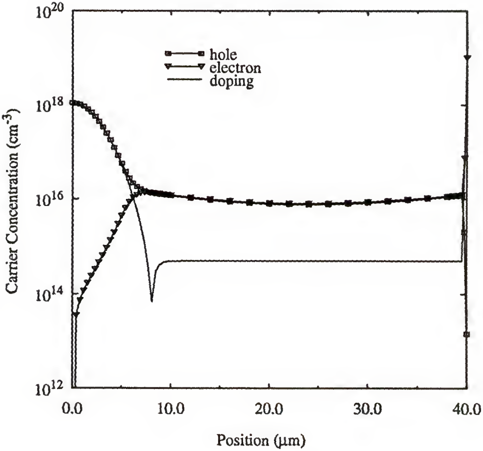


Figure 2.13 PISCES simulated carrier concentrations in the reverse-mode operation (V_{DS}=-1V, along y axis), compared with the background doping concentration.

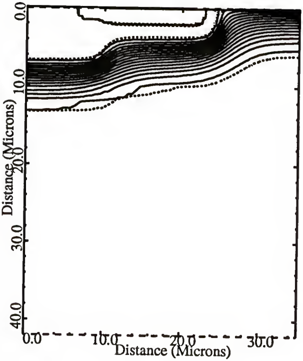
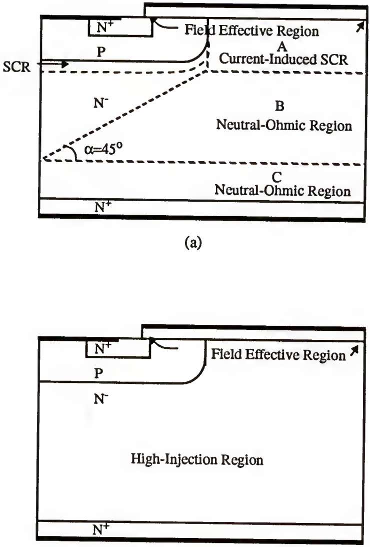


Figure 2.14. PISCES simulated potential distribution in Off-State (V_{GS}=0V, V_{DS}=25V).

from the transient displacement current of the P-body/N-epi junction at high dV_{DS}/dt or the reverse recovery current when the holes are released from the high injected N-epi region. The up-mode BJT (with $n^-/p/n^+$ as Emitter/Base/Collector) is on in the reverse bias operation because the N-epi/P-body junction is forward-biased and the P-body/N-source junction is shorted. Turning on the down-mode BJT during a transient is destructive to the device. Neglecting the effect of the parasitic BJT is essential for the device design.

2.5 Summary

The device simulations of the VDMOST suggests that the device has a field-effective channel region, a segmented drift region, and a space-charge region at the P-N junction as shown in Fig. 2.15(a). The MOS channel region at the surface of the device under the poly gate extends from the overlapped N^+ source, P-body, and the N-epi regions. According to the current flowlines, the drift region can be segmented into a rectangular region A, a trapezoidal region B, and a rectangular region C. Region B and C are uniformly doped neutral-ohmic regions where majority carrier concentrations are about the background doping. Region A is a current-induced space-charge region in quasi-saturation operation when the excess electrons and high field gradient are observed. The drift region becomes a high-injection region during reverse operation where the electron and hole concentrations are about equal and much higher than the background doping.



(a)

(b)

Figure 2.15 Regions of the VDMOST, (a) in forward and (b) in reverse operating conditions.

Having the regions well identified, the regional models are ready to be derived using the rules in section 2.2, as will be discussed in the next chapter.

CHAPTER 3
MODEL DEVELOPMENT

As described in the previous chapter, physical models for power devices are developed via a regional approach by dividing the devices into basic regions such as a quasi-ohmic region, a space-charge region, a high-injection region, a MOS channel region, or a current-induced space-charge region. The VDMOST is a good example for a physical model because it contains all the regions listed above. It has unipolar and bipolar device performance in forward and reverse operation, respectively, as described in the previous chapter.

In the first section, the VDMOST model is developed based on two-dimensional PISCES simulations. Section 3.2 and 3.3 describe a more precise model for the VDMOST that accounts for the reverse-recovery of the parasitic PIN diode and the 3-D structure, respectively. In the last section, the temperature-effect equations for the model parameters, important for power devices, are listed.

3.1 VDMOST Model

Driven by insight afforded by PISCES simulations, the device can be divided into a channel region, a segmented drift region, a parasitic BJT device, parasitic charges, and a PIN diode for reverse operation. The model for the double-diffused channel region can be used in LDMOS, IGBT, MCT, and other devices with the same channel structure. The model is based on [KIM90] with the following modifications: 1) the network representation is modified to reflect the PISCES simulations by moving the terminal of the body/epi junction charging term to the end of Region A; 2) a series resistance is introduced that accounts for the resistance in the drain buried layer for the updrain structure and can be extracted from the reverse mode current-voltage characteristics; 3) 3-D device simulation (TMA DAVINCI) is completed for a cell structure instead of the 2-D structure resulting in the definition of more realistic structural areas for input parameters; 4) a parasitic PIN diode is used which includes reverse-recovery effect instead of the up-mode transistor in the old model; 5) the gate capacitances in all the operating regions are fully considered; 6) the old channel model lacked subthreshold characteristics, so that a SPICE model level-3 steady-state current equation (which has subthreshold characteristics) is also implemented as a user selective channel model; 7) the old channel model has the velocity saturation at the source end, and the new model is extended to account for the saturation at the drain end, too; 8) an effective electron concentration is introduced in JFET region which describes the quasi-saturation behavior and reduces an internal loop in the circuit model; 9) temperature-dependence is included in the model; and 10) the model is implemented in two circuit simulators: Saber and SPICE2G6.

Based on the two-dimensional PISCES simulation, the VDMOST is partitioned into several regions and parasitic components as described in the previous chapter. Figure 3.1 shows the VDMOST structure with its geometric parameters. The channel and the segmented drift region are the main current

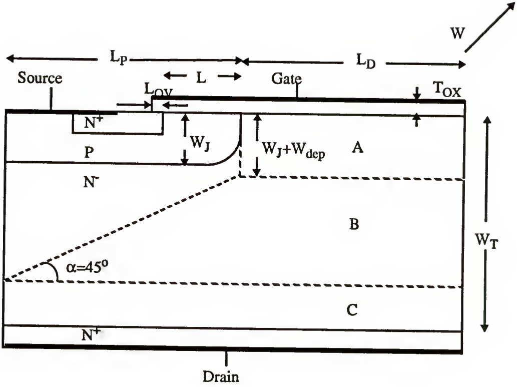


Figure 3.1 The structure and the geometric parameters of a VDMOST. The drift region is segmented into three sub-regions according to the current flowlines in the PISCES simulations.

path in forward operation. For the reverse bias operation, the P-body/N-epi/N$^+$ buried layer forms a PIN diode. Charges that contribute to the transient current have to be included in the model, too. A large junction charge appears at the P-body/N-epi junction. The gate charges include all the charge under the gate in the N-source, the P-body, and the N-epi regions. Besides, the parasitic BJT can turn on in transient operation, and it is also included in the model.

This section describes the equations used in quasi-2-D model for all the regions in the VDMOST.

3.1.1 Channel Region

In [KIM90], for numerical simplicity, the non-uniform doping density along the channel is approximated as an exponential function of the position x

$$N_A(x) = N_{A0} exp\left(-\frac{\eta x}{L}\right) \tag{3.1}$$

where N_{A0} is the peak doping, L is the channel length, and $\eta = ln(N_{A0}/N_D)$ is the doping gradient. The strong-inversion channel current with a field-effective mobility can be written as

$$I_{CH} = \frac{W\mu_n\left(Q_{n0}^2 - Q_{nL}^2\right)}{2L(C_{OX} + C_D)\left(1 + \frac{\mu_n}{2Lv_{sat}}V_{CH}\right)} \tag{3.2}$$

where V_{CH} is the channel voltage drop, v_{sat} is the electron saturated velocity, and (μ_n is the electron mobility affected by the transverse field$\mu_n = \mu_{n0}/(1+\theta(V_{GS}-V_{TH}))$, with μ_{n0} is the low-field electron mobility, V_{TH} is the threshold voltage, and θ is the fitting parameter that defines the transverse-field dependence.). Q_{n0} and Q_{nL} are the inversion charge at the source end and the drain end of the channel, respectively,

$$Q_{n0} = -C_{OX}(V_{GS}-V_{TH}) \tag{3.3}$$

$$Q_{nL} = -C_{OX}\left(V_{GS}-V_{TH}-V_{CH}\left(1+\frac{C_D}{C_{OX}}\right)\right) \tag{3.4}$$

$C_{OX} = \varepsilon_{SO}/T_{OX}$, is the oxide capacitance. The depletion capacitance C_D, is assumed to be invariant along the channel

$$C_D = C_{D0}\left(1-\frac{2\eta|\phi_B|}{V_{CH}}\right) \tag{3.5}$$

where $C_{D0} = \sqrt{-q\varepsilon_s N_{A0}/4\phi_B}$, with $\phi_B = -V_t ln(N_{A0}/n_i)$, n_i is the intrinsic carrier concentration, and V_t is the thermal voltage.

If the saturation of the VDMOS current is due to the electron velocity saturation at the source end of the channel as in [KIM90], the saturation current is

$$I_{CH(sat)} = -Wv_{sat}Q_{n0} \tag{3.6}$$

By equating (3.2) and (3.6), the saturation channel voltage can be found

$$V_{CH(sat)} = \frac{A - \sqrt{A^2 - 8Lv_{sat}C_{OX}(V_{GS} - V_{TH})(C_{OX} + C_{DO})/\mu_n}}{2(C_{OX} + C_{DO})} \tag{3.7}$$

where $A = C_{OX}(V_{GS} - V_{TH}) + 2\eta C_{DO}\phi_B$.

It is also possible for electrons to saturate at the drain end of the channel. If this is the case, the saturation current is

$$I_{CH(sat)} = -Wv_{sat}Q_{nL} \tag{3.8}$$

Then the saturation channel voltage is obtained by equating (3.2) and (3.8)

$$V_{CH(sat)} = \frac{C_{OX}(V_{GS} - V_{TH}) + 2\eta C_{DO}|\phi_B|}{\mu_n C_{OX}(V_{GS} - V_{TH})/(2Lv_{sat}) + C_{OX} + C_{DO}} \tag{3.9}$$

The channel gradient and the length determine whether saturation occurs at the source or at the drain end. Since the channel current is mostly drift current, the lower the electron charge at a point, the higher the electron velocity (v_n) at the position ($I = WQ_n(x)v_n$). The velocity saturation occurs at the drain end if $Q_{nL(sat)} < Q_{nO}$. With (3.3),(3.4), and (3.9), the condition becomes

$$\frac{Lv_{sat}}{\mu_n} > \frac{\eta|\phi_B|}{1 + \frac{C_{OX}}{C_{DO}}} \tag{3.10}$$

If the condition in (3.10) holds, the electron velocity saturates at the drain end, otherwise, it will be at the source end. As the channel length L increases and the channel gradient η decreases, the velocity saturates at the drain end. This agrees with the extreme cases discussed in the previous section.

When $V_{CH} < V_{CH(sat)}$ (with $V_{CH(sat)}$ given by (3.7) or (3.9)), the device is in the linear operating region, and the channel current is given by (3.2). Otherwise, the current is given by (3.6) or (3.8), when the device is in the saturation region.

3.1.2 Drift Region

As in [KIM90] and from PISCES simulations of the current flowlines, the drift region is divided into a rectangular region A, a trapezoidal region B, and a rectangular region C (Fig. 3.1) under normal operations. Region A is a current induced-space-charge region, so that the current equation and the Poisson's equation are both used to obtain the voltage drop. However, the old model has two complicated implicit equations, which require more inner iterative loops when implementing the model into circuit simulators. It is modified in this work by interpolating between the solutions for the low-field and the high-field conditions. The current equation in (2.9) which incorporates the field-effective mobility model can be written as

$$I_D = A_a q N_D \mu_{nd} E_y,\ \text{if } E_y \ll E_C \tag{3.11}$$

$$I_D = A_a q n v_{sat},\ \text{if } E_y \gg E_C \tag{3.12}$$

where $A_a = WL_D$ is the effective area in Region A. According to PISCES simulations, in the linear and the low-field conditions, the electron concentration in Region A is about the same as the background doping except at the surface under the gate where the accumulation layer is. When in quasi-saturation, there is a high-field in Region A causing the saturation of the electron velocity, the current can only be increased by raising the electron concentration level. The excess electrons in Region A form a space-charge layer that support the gradient of the field as illustrated in Poisson's equation. Equation (3.12) gives the relation of the electron concentration with the current in this situation. The electron concentration depends heavily on the current level. An effective electron concentration is introduced with respect to I_{AS}, the onset current of the velocity saturation,

$$N_{eff} = \frac{I_D}{A_a q v_{sat}},\ \text{if } I_D > I_{AS}(1 + f_{neff})$$

$$= N_D + f_{neff} N_D \exp\frac{(I_D/I_{AS} - 1 - f_{neff})}{f_{neff}},\ \text{otherwise} \tag{3.13}$$

where $I_{AS} = A_a q N_D v_{sat}$, f_{neff} is an empirical parameter which is needed to link N_{eff} in the low-current and the high-current regions. Note that when the current is much lower than the critical current I_{AS}, N_{eff} approaches N_D. If the current is high, N_{eff} will approx-

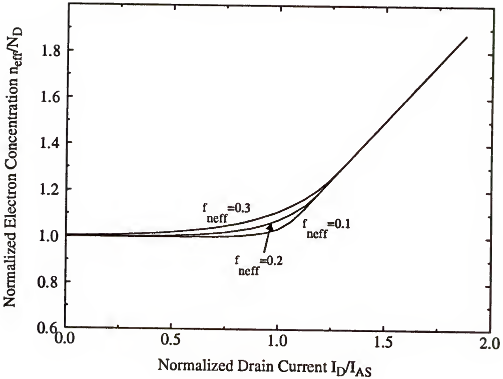


Figure 3.2 The normalized effective electron concentration vs. the normalized drain current with different fitting parameter f_{neff}.

imate $I_D/A_a q v_{sat}$, which agrees with the theory. It is shown in Fig. 3.2 as respect to I_D with different value of f_{neff}. The extraction of this parameter is discussed in Chapter 4. A moving boundary at the bottom of Region A is assumed according to PISCES simulation

$$W_A = W_J + W_{dep} \tag{3.14}$$

where W_{dep} is the depletion width of the P-N junction and by the depletion approximation

$$W_{dep} = \sqrt{\frac{2\varepsilon_s (V_{CH} + V_A)}{qN_D}} \tag{3.15}$$

The voltage drop across Region A for the low-field condition can be solved using the current equation(3.11). For the high-field condition (after velocity saturates), excess carriers causing the field gradient which is described by the Poisson's equation. V_A of this effect can be obtained by Poisson's equation(2.10) using the effective electron concentration, which can be written as

$$V_A = \frac{I_D W_A}{A_a q N_{eff} \mu_{nd}} + \frac{q}{2} (N_{eff} - N_D) W_A^2 \tag{3.16}$$

The first term is the low-field solution when $N_{eff} = N_D$. The second term becomes significant at high field in Region A when the current is high.

In Region B, the current flows down under the body with an angle of α (=45°). V_B and V_C can be obtained by solving E_y in (2.9) and integrating to obtain the voltage drops as suggested in [KIM90]

$$V_B = \frac{I_D \tan\alpha}{WqN_D\mu_{nd}} \ln \frac{WqN_D\mu_{nd}(L_D + L_P) - \frac{I_D}{E_c}}{WqN_D\mu_{nd}L_D - \frac{I_D}{E_c}} \qquad (3.17)$$

$$V_C = \frac{I_D(W_T - W_J - W_{dep} - L_p \tan\alpha)}{W(L_P + L_D)\, qN_D\mu_{nd} - \frac{I_D}{E_c}} \qquad (3.18)$$

The channel region and the drift region models complete the steady-state active components of the VDMOST.

3.1.3 Charges

During the transient turn-on and turn-off, the gate charges and the junction charge contribute to the current in the VDMOST. Using the quasi-static approximation, the transient charge current in branch i can be expressed as

$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i dV_j}{\partial V_j dt} \qquad (3.19)$$

where Q_j and V_j denotes the charge and the voltage across terminal branch j.

Ong et. al. considered seven operating regions for the gate charge [ONG91][BUD92]. They observed that the gate charge is due to the charge under the gate in both the channel and the drift regions. Each of these two regions can be separately in either accumulation, depletion, or inversion state. Thus, seven possible combinations are obtained. They assumed the channel charge contributes to the gate/source capacitance and the drift-region charge contributes to the gate/drain capacitance. However, the channel charge should be partitioned between both the source and the drain end for MOSFETs [TSI88]. Also, the charge from gate electrode overlapping the source cannot be neglected [KIM90][HEF88]. Thus, the gate source charge is

$$Q_{GS} = -Q_{OV} - \frac{1}{2} Q_{CH} \tag{3.20}$$

where $Q_{OV} = WL_{OV}C_{OX}V_{GS}$, is the charge in the gate/source overlapping region, with L_{OV} is the overlapping length. Q_{CH}, the channel charge, is either from channel accumulation, depletion, or inversion charge

$$\begin{aligned} Q_{CH} &= -WLC_{OX}(V_{GS} - V_{FBP}) \text{ , if } V_{GS} < V_{FBP} \\ &= Q_{CHD}\text{, if } V_{FBP} < V_{GS} < V_{TH} \\ &= -WLC_{OX}(V_{GS} - V_{TH}) + Q_{CHDO}\text{, if } V_{GS} > V_{TH} \end{aligned} \tag{3.21}$$

where V_{FBP} is the channel region flatband voltage, Q_{CHD} is the channel depletion charge and is given by the depletion approximation

$$Q_{CHD} = -WL\sqrt{2q\varepsilon_s N_A \Psi_{sp}} \tag{3.22}$$

where ψ_{sp}, the surface potential can be obtained by the basic MOS equation

$$V_{GS} - V_{FBP} = \psi_{sp} + \frac{Q_{CHD}}{WLC_{ox}} \tag{3.23}$$

Note that when the channel is in inversion, Q_{CH} includes an inversion charge and a constant depletion charge $Q_{CHDO} = Q_{CHD}\big|_{V_{GS} = V_{TH}}$ because the surface potential is pinched.

The gate/drain charge Q_{GD} includes the charge in the drift region under the gate and the partitioned channel charge,

$$Q_{GD} = -Q_{CHN} - \frac{1}{2}Q_{CH} \tag{3.24}$$

where Q_{CHN} is the charge in the drift region under the gate. As Q_{CH}, it can be either accumulation, depletion, or inversion charge during normal operation.The effective gate/drain capacitance is amplified by the Miller effect, thus slowing down the gate-controlled switching. The basic MOS theory indicates the accumulation layer forms when $V_{GS} - V_{CH} - V_{FBN} > 0$. and is

$$Q_{CHN} = -A_a C_{OX}(V_{GS} - V_{CH} - V_{FBN}) \tag{3.25}$$

where V_{FBN} is the gate/epi-region flatband voltage. A depletion region forms when $V_{GS} - V_{CH} - V_{FBN} < 0$. The charge is given by the depletion approximation

$$Q_{CHN} = A_a\sqrt{2q\varepsilon_s N_D(-\psi_{sn})} \tag{3.26}$$

where ψ_{sn} is the surface potential given by

$$V_{GS} - V_{CH} - V_{FBN} = \psi_{sn} + \frac{Q_{CHN}}{A_a C_{OX}} \tag{3.27}$$

If the gate voltage is very low, it is possible that an inversion layer forms under the gate in the drift region. If this is the case, then Q_{CHN} becomes

$$Q_{CHN} = -A_a C_{OX} (V_{GS} - V_{CH} - V_{THN}) + Q_{CHN0}, \text{ if } V_{GS} - V_{CH} - V_{THN} < 0 \tag{3.28}$$

where Q_{CHN0} is the depletion charge at $V_{GS} - V_{CH} = V_{THN}$ and V_{THN} is the threshold voltage needed for an inversion layer to form at the surface of the drift region.

The junction charge comes from the depletion of the P-body/N-epi junction, and the area of the junction includes both the bottom and the sidewall part of the junction. It is again obtained by the depletion approximation

$$Q_J = qW(L_P + W_J) N_D W_{dep} \tag{3.29}$$

3.1.4 Parasitic Devices

As described in the previous section, a parasitic BJT exists (N^+-source/P-body/N^--epi) in the VDMOST. Since P-body contact is shorted to the source contact, the parasitic BJT is off during normal operation. However, due to the existence of p-body resistance, a large transient current flowing through the region can cause a sufficient voltage drop in P-body region to forward bias the source/body junction and to make the parasitic device turn-on [MOH89]. The transient current can either be the displacement current from the originally depleted P-body/N-epi junction or the reverse recovery current from the high-injection N-epi region. High dV_{DS}/dt causing the displacement current and high reverse recovery current should be avoided to prevent the turning on of the parasitic BJT. In the model, the parasitic BJT is modeled by a conventional BJT current equation

$$I_{CT} = I_{CES}exp\left(\frac{V_{BE}}{V_t}\right) - I_{CCS}exp\left(\frac{V_{BC}}{V_t}\right) \tag{3.30}$$

where I_{CES} and I_{CCS} are the saturation currents of the parasitic BJT. V_{BE} and V_{BC} are the voltage drops across the P-body/N-source and P-body/N-epi junctions, respectively. Note that when the VDMOST is reverse-biased, the P-body/N-epi junction is forward-biased, then the BJT is in reverse-active operation.

When VDMOST is in the reverse mode, except for the turning on of the reverse-active parasitic BJT, a large portion of the current flows through the P-body/N-epi/N-drain diode. As described in the previous section, the n-epi region is in high injection. The P-I-N diode current also provides the base current for the reverse active parasitic BJT. The current can be obtained by solving the current equation with the continuity equation. The solution, simplified in [GHA77], is

$$I_R = \frac{2WqD_a n_i}{d} F(d)\, exp\left(-\frac{V_{DS}}{f_m V_t}\right) \tag{3.31}$$

where D_a is the ambipolar diffusivity, $d = (W_T - W_J)/2$ is half the distance of the epi-region, f_m is the fitting parameter with a value between 1 and 2. $F(d)$ is

$$F(d) = \frac{d}{L_a} tanh\left(\frac{d}{L_a}\right)\left(1 - B^2 \frac{d}{L_a}\left(tanh\left(\frac{d}{L_a}\right)\right)^4\right) exp\left(-\frac{V_m}{V_t}\right) \tag{3.32}$$

where $L_a = \sqrt{D_a \tau}$ (τ the high injection life time), is the ambipolar diffusion length. B is $(\mu_n - \mu_P)/(\mu_n + \mu_p)$. V_m is the voltage drop across the epi-region which is

$$V_m = \frac{3}{2} V_t \left(\frac{d}{L_a}\right)^2 \tag{3.33}$$

The carrier charge in the epi-region which contributes to the transient current is obtained by

$$Q_p = I_R \tau \tag{3.34}$$

The model also includes a drain (N^+ region) resistance R_d because the current usually travels far in the N^+ region before entering drain contact in the up-drain structures. It can be extracted from the I_{DS}-V_{DS} characteristics in the reverse operating region since R_d is approximately the reverse-mode on-resistance.

This concludes the discussion of basic VDMOST model. A circuit representative for the model is shown in Fig. 3.3. It is based on the 2-D device struc-

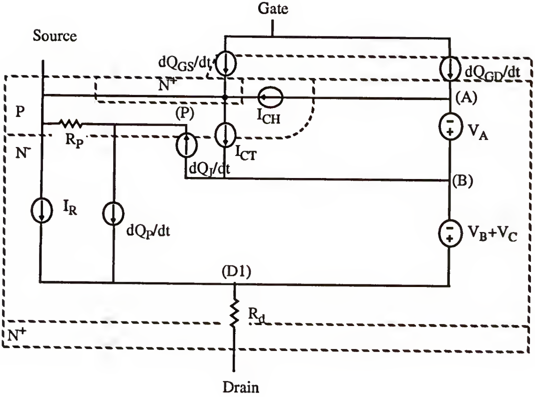


Figure 3.3 Circuit representation of the VDMOST model imposed on the device.

ture and the quasi-static approximation for all the charges. For a more precise model, the 3-D structure and the non-quasi-static assumption should be considered as discussed in the next two sections.

3.2 Parasitic Diode with Reverse-Recovery Current

When the drain voltage is negative, the parasitic diode turns on. As described in Chapter 2, the diode resembles the PIN diode which operates in high-level injection. The reverse-recovery of the parasitic PIN diode is an important effect for the MOSFET. It delays the circuit operation and can turn-on the parasitic BJT. When the diode is turned-off from its on-state, a large reverse-recovery current is observed as shown in Fig. 3.4. The peak reverse-recovery current I_P will increase with higher switching speed. The quasi-static assumption in the previous section is not good enough to describe the charge redistribution in the low-doped region. There are many PIN diode models [LIA90] [LAU91], among them [LAU91] is a simple diode model including reverse recovery which is important for the VDMOST. It uses a lumped charge concept and rewrites the continuity equation in terms of charge

$$0 = \frac{dQ_M}{dt} + \frac{Q_M}{\tau} - \frac{Q_E - Q_M}{T_M} \tag{3.35}$$

where T_M is the transit time, τ is the carrier lifetime, Q_M is the charge in the low-doped region, and Q_E is the junction charge variable which is

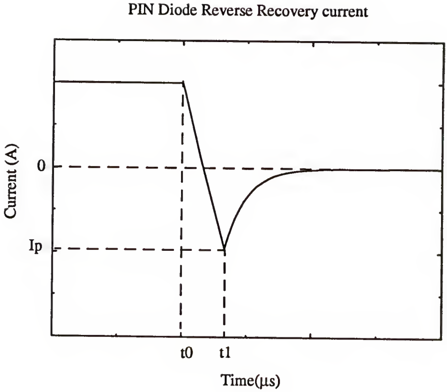


Figure 3.4 The reverse-recovery current for the parasitic PIN diode in the VDMOST

$$Q_E = I_{RS}\tau exp\left(\frac{-V_{DS}}{f_m V_T} - 1\right) \tag{3.36}$$

where I_{RS} is the diode saturation current and f_m is the emission coefficient. Then the diode current which includes both the steady-state and the transient current is

$$I_R = \frac{Q_E - Q_M}{T_M} \tag{3.37}$$

There are four parameters in this diode model, I_{RS}, f_m, T_M, and τ. The first two parameters can be extracted from the steady-state I-V curve in reverse operation. The later two parameters can be determined from the transient reverse-recovery current waveform, as will be discussed in Chapter 4.

3.3 Modifications for Three-Dimensional Structure

The quasi-2-D model is good for comparison with 2-D device simulation result, however, it can not account for a real device because of the nonuniform structure in the third dimension of the device. Instead of using an effective device width to calculate the VDMOST component areas, real effective areas should be used to calculate all the current and voltage components in the VDMOST. Figure 3.5 shows the top view of a VDMOST with a magnified quarter cell.

Three-dimensional device simulation is done by using TMA DAVINCI on a quarter of a cell. Figure 3.6 shows the VDMOST constructed for 3-D device

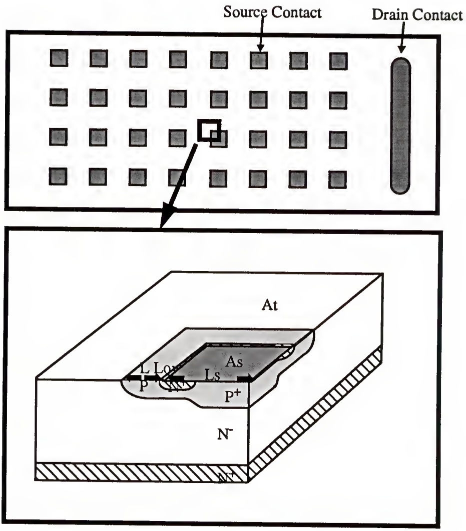


Figure 3.5 The top view of a VDMOST. A quarter of a cell is shown microscopically with the geometric parameters.

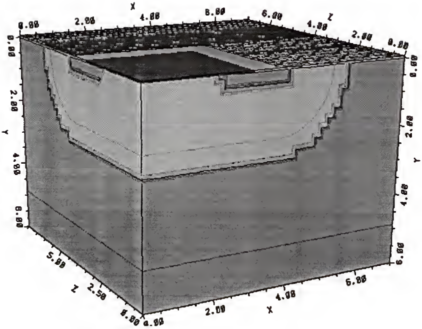


Figure 3.6 The VDMOST structure for three-dimensional device simulation.

simulations. For the square shape source window, the electrons flow both in the x and z direction into the channel, through the drift region and are collected in the N^+ buried layer. The area of Region A is the total area subtracting the P-body area. Region B has the current spreading in both x and z direction. Figure 3.7 shows the current magnitude in the cross-section along the y-axis. The current cross-sectional area of Region B can be assumed to be rectangular by subtracting a smaller rectangular area as illustrated in Fig. 3.8(a). Compare this with KIM's model in Fig. 3.8(b). For the model herein, the cross-sectional area is a function of y due to current spreading and is

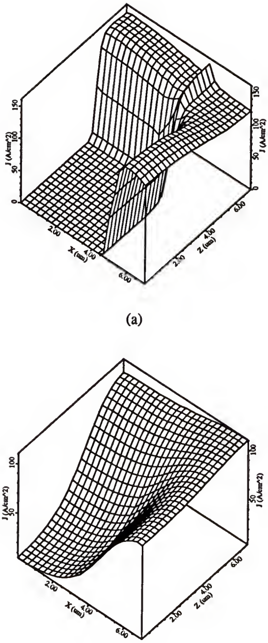
$$A_y = A_T - A_P (1 - y/L_P)^2 \text{ at position y} \tag{3.38}$$

Note that $A_y = A_T - A_P$ at the top of Region B and $A_y = A_T$ at the bottom of Region B. A $45°$ current spreading angle is still assumed. Thus, the voltage drop across this region becomes

$$V_B = L_P \frac{KE_c}{2\sqrt{A_p (A_T - K)}} \ln \frac{\sqrt{\frac{A_T - K}{A_P}} + 1}{\sqrt{\frac{A_T - K}{A_P}} - 1} \tag{3.39}$$

where $K = I_D / (q N_D \mu_{nd} E_C)$.

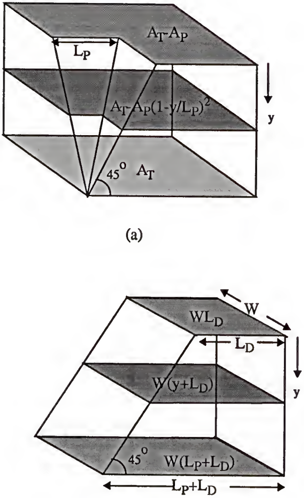
Table 3.1 shows the effective areas of the components for the 2-D and 3-D models. Instead of the effective width and lengths for the structure, the 3-D



(a)

(b)

Figure 3.7 Current magnitude at the planes (a) y=2μm and (b) y=4μm.



(a)

(b)

Figure 3.8 Effective area of Region B in (a) the 3-D structure model and (b) KIM's model.

Table 3.1: Comparison of the 2-D and 3-D components' effective areas and lengths.

Components	2-D	3-D
Input	L_S, L_D, W	A_S, A_T, N
I_{CH}	W	W^a
V_A	WL_D	$A_T - A_P$
V_B	$W(L_D + y)$	$A_T - A_P(1 - y/L_P)^2$
V_C	$W(L_P + L_D)$	A_T
Q_J	$W(L_P + W_J)$	$2L_PW_J + A_P^b$
Q_{GS}	WL_{OV} WL	$A_S(1 + L_{OV}/L_S)^2 - A_S$ $A_P - A_S(1 + L_{OV}/L_S)^2$
Q_{GD}	WL_D WL	$A_T - A_P$ $A_P - A_S(1 + L_{OV}/L_S)^2$
Q_P	WL_P	A_P
I_{CT}	W	N
I_R	WL_P	A_P

a. The channel width is $2L_S$ and $L_S = A_S^{0.5}$ for square source contact.

b. $A_P = A_S(1 + (L + L_{OV})/L_S)^2$

structure uses areas and the number of cells as input parameters. The area of Region A is $A_T - A_P$ instead of WL_D. The same reasoning is used for other components as listed in the table. The equations for the 3-D structure can be obtained by replacing the 2-D effective area terms with the 3-D effective area terms. The voltage drop in the drift region B (V_B) is rederived for the quasi-3-D model (3.39) and has a different form as with the 2-D model.

3.4 Temperature-Dependent Parameters

The operating temperature has a profound effect on device performance. Temperature-dependent parameters have to be modified when the device temperature is not equal to the nominal temperature. This temperature-dependent parameters includes the thermal voltage V_t, the electron mobilities μ_{n0} and μ_{nd}, the electron saturation velocity v_{sat}, the threshold voltage V_{TH}, the energy gap E_g, the electron and hole masses m_n and m_p, the intrinsic carrier concentration n_i, the parasitic resistances R_d and R_p, and the diode saturation current I_{RS}, as listed below [HEF92]

$$V_t = \frac{KT}{q} \tag{3.40}$$

$$\mu_{n0} = \mu_{n00}\left(\frac{T_{nom}}{T}\right)^{2.5} \tag{3.41}$$

$$\mu_{nd} = \mu_{nd0}\left(\frac{T_{nom}}{T}\right)^{2.5} \tag{3.42}$$

$$v_{sat} = v_{sat0}\left(\frac{T_{nom}}{T}\right)^{0.87} \tag{3.43}$$

$$V_{TH} = V_{TH0} - f_{vth}(T - T_{nom}) \tag{3.44}$$

$$E_g = 1.179 - 9.025\left(10^{-5}\right)T - 3.05\left(10^{-7}\right)T^2 \tag{3.45}$$

$$m_n = 1.034 + 5.826\left(10^{-4}\right)T + 2.826\left(10^{-7}\right)T^2 \tag{3.46}$$

$$m_p = 0.552 + 1.1\left(10^{-3}\right)T + 7.769\left(10^{-7}\right)T^2 \tag{3.47}$$

$$n_i = 4.9e15\,(m_n m_p)^{0.75}T^{1.5}exp\left(-\frac{E_g}{2KT}\right) \tag{3.48}$$

$$I_{RS} = I_{RS0}exp\left(-\frac{qE_g}{K}\left(\frac{1}{T} - \frac{1}{T_{nom}}\right)\right) \tag{3.49}$$

$$R_d = R_{d0}\left(\frac{T}{T_{nom}}\right)^{2.5} \tag{3.50}$$

$$R_p = R_{p0}\left(\frac{T}{T_{nom}}\right)^{2.5} \tag{3.51}$$

where T is the operating temperature and T_{nom} is the nominal temperature at which the parameters are extracted. K is the Boltzmann constant. The parameters in the right-hand side of the equations with '0' subscript denote the nominal temperature value, and the left-hand side terms are the temperature modified values. The threshold shifting parameter f_{vth} can be obtained with the measurement of the threshold voltage in different temperatures, as will be discussed in Chapter 4.

3.5 Summary

In this chapter, the VDMOST model is described in detail. This model is based on the physical circuit model developed by Kim and Fossum, with modifications that is either more physical or more suitable to be implemented in circuit simulators. In this work, a realistic cell structure is considered instead of a quasi-two-dimensional structure as in the previous work. Also, the non-quasi-static effect resulting in the reverse-recovery for the parasitic PIN diode and the temperature dependence that is important for the power devices are incorporated. The next section describes the implementation of this model and the method to obtain the model parameters.

CHAPTER 4
MODEL IMPLEMENTATION, VERIFICATION AND PARAMETER EXTRACTION

In this chapter, the VDMOST model, described in Chapter 3, is implemented in circuit simulators Saber and SPICE2G6. A system interfacing ICCAP, Saber, and the measurement equipment is set up for measurements, simulations, and parameter extractions for the model. The model is further verified with the test circuits recommended by NIST, as examples for the model template applications.

4.1 Model Implementation

The physical VDMOST model is implemented in Saber and SPICE2G6. The Saber simulator [MAS90] offers independent model development capability better than any other circuit simulators. A physical device model with internal nodes and implicit equations can be written easily into a Saber template by using MAST modeling language without changing other subroutines as with SPICE. However, SPICE is more popular for circuit designers. There is still a great need for SPICE models for power devices.

The circuit representation of the VDMOST (Fig. 3.3) includes both current and voltage sources with three external nodes (D,G,S) and four internal nodes (A,B,P,D1). Input parameters are either device parameters or model parameters. Device parameters are layout-dependent and thus can differ from device to device on the same IC chip. Model parameters are process-dependent and generally common to all the VDMOS devices on the same chip.

The Saber model is written in MAST language. The MAST modeling language can represent a model in terms of linear or nonlinear algebraic or integral-differential equations. The Saber simulator can then access these models. A complete MAST description of an element, subsystem, or entire system is contained in a file and is called a template.

The VDMOST template, like the other Saber templates, contains a template header, header declarations, local declarations, a parameter section, a value section, a control section and a equation sections. The template header declares the name of the template, the connection points, and the arguments. It determines how to refer to a template as a netlist entry. The header declaration section specifies the external connection points and argument names given in the header and their default values. The VDMOST input parameters are defined here so that they can be extracted when linking with ICCAP. The local declarations section specifies any other variables used locally within the template. The parameters section is used to manipulate parameters. The values section provides informations for the equations section. The control section defines the information for the numerical iteration. Finally, the equation section lists the intrinsic equations to be solved and constructs the model netlist defining branch equations with current sources or voltage sources.

The Saber simulator requires an input file containing a netlist that completely describes the system in the MAST language. To start simulating the VDMOST template, an input file that contains only a VDMOST device and independent voltage sources V_{GS} and V_{DS} is constructed and simulated under steady-state and transient conditions. Figure 4.1 shows the simulation result of the steady-state I_D-V_{DS} characteristics compared with PISCES results. In Figure 4.2, the transient drain and gate current obtained by turning off the gate voltage while a constant V_{DS} is given. The comparison with the simulation result is limited by PISCES circuit interconnect ability with other circuit elements. Both of them show good agreement with the PISCES simulation.

The SPICE implementation requires that all dependent sources be functions of nodal voltages (and not branch currents) since the nodal voltages are the independent variables in SPICE. Therefore, the current-dependent voltage sources are converted to voltage-dependent current sources for SPICE implementation. The equivalent circuit, re-derived for the SPICE implementation, is shown in Fig. 4.3. Note that the two terms in V_A (3.16) are arranged into two current sources I_{A1} and I_{A2} in series, where

$$I_{A1} = \frac{qWL_D\mu_{nd}N_D V_{LA}}{W_J\sqrt{1-\frac{\left(\frac{\mu_{nd}V_{LA}}{W_D}\right)^2}{v_{sat}^2}}}, \text{ if } \mu_{nd}V_{LA}/W_J < v_{sat}$$

$$= \frac{100qWL_D\mu_{nd}N_D V_{LA}}{W_J}, \text{ otherwise} \qquad (4.1)$$

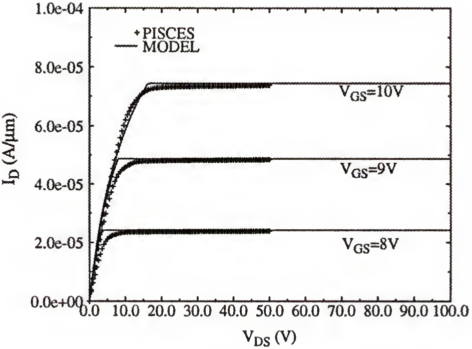


Figure 4.1 Steady-state drain current vs. drain voltage simulations compared with PISCES result.

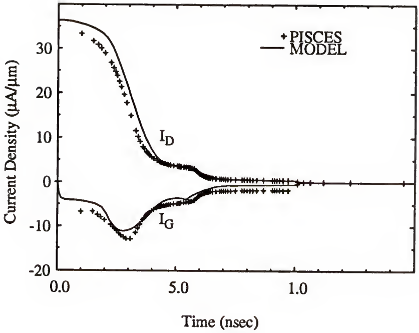


Figure 4.2 Drain and gate current during VDMOST turn-off for the 2-D model compared with PISCES simulation (V_{DS}=5V, V_{GS} switches from 7V to 0V with fall time 10 nano seconds).

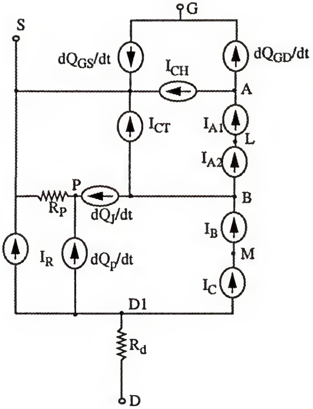


Figure 4.3 Circuit representation for SPICE implementation. Note that the voltage sources (in Fig. 3.3) are converted to the current sources.

$$I_{A2} = qWL_D v_{sat}\sqrt{\left(\frac{\varepsilon_s V_{BL}}{qW_J^2}\right)^2 + 2N_D\left(\frac{\varepsilon_s V_{BL}}{qW_J^2}\right)},\ \text{if}\ \left(\frac{\varepsilon_s V_{BL}}{qW_J^2}\right) > 0.01N_D$$

$$= 14.1774qWL_D v_{sat}\left(\frac{\varepsilon_s}{qW_J^2}\right)V_{BL},\ \text{if}\ \left(\frac{\varepsilon_s V_{BL}}{qW_J^2}\right) < 0.01N_D \qquad (4.2)$$

where V_{LA} and V_{BL} are the voltage drops across the nodes L,A and B,L respectively.

The quasi-3-D model is implemented in Saber, too. One more feature of this implemented model is the user selectable channel models. The SPICE MOSFET model level-3 for the steady-state characteristics [ANT88] is also implemented as a level-0 in the VDMOST model. The advantage of using the SPICE channel model is that it includes subthreshold characteristics unlike Kim's model (implemented as level-1) described in the previous chapter.

For the physical VDMOST model, input parameters are either structural (Table 4.1) or extracted model parameters (Table 4.2). T_{OX}, W_T, W_J, N_{AO}, N_D, L, L_{OV}, A_S, A_T, and N are structural parameters. T_{OX}, W_T, W_J, N_{AO}, and N_D can be obtained from measurement by probing the resistance along a cut inside the device with a bevealled angle, so that the doping can be calculated from the resistance. A_S and A_T, the source and total quarter cell area, are obtained from the layout information. L and L_{OV}, the channel length and the source/gate overlap length, are obtained from the body and N^+ source junction depth multiplied by a lateral diffusion factor 0.8.

The number of quarter cells N is used to scale up the currents from the cell level, and is the product of the number of fingers times the number of the

Table 4.1: VDMOST structural parameters

Name	Description	Default	Unit
T_{OX}	Gate oxide thickness	10^{-4}	μm
W_T	Substrate thickness	20	μm
W_J	Body junction thickness	6.4	μm
N_{A0}	Channel peak doping	10^{17}	cm^{-3}
N_D	Epi-region doping	$1.1\ 10^{15}$	cm^{-3}
L	Channel length	1.8	μm
L_{OV}	Source/gate overlap length	0.3	μm
A_S	Source contact area	36	μm^2
A_T	Total cell area	180	μm^2
N	Number of cells	200	-

Table 4.2: VDMOST model parameters

Name	Description	Initial	Unit
f_m	Reverse current fitting factor	2.	-
I_{RSO}	Reverse diode saturation current	1e-11	A
R_{d0}	Drain buried-layer resistance	2.	Ω
V_{TH0}	Threshhold voltage	1.5	V
μ_{n00}	Channel low-field mobility	1350	$cm^2/V{\bullet}sec$
μ_{nd0}	Drift-region low-field mobility	1350	$cm^2/V{\bullet}sec$
θ	Transverse field fitting factor	0.	-
f_{neff}	Region A effective-electron-concentration factor	0.3	-
f_{ns}	Subthreshold current factor	5	–
W	effective channel width	$2L_S$	μm
v_{sat0}	channel saturation velocity	1e5	m/sec
f_{sh}	short-channel effect factor	0.3	-
f_{qja}	junction-charge area factor	1.	-
f_{qga}	gate-charge effective area factor	1.	-
V_{THN}	Epi region inversion threshold voltage	-4	V
f_{vth}	threshold voltage thermal factor	9e-3	-
T_M	PIN diode carrier transit time	5.	μsec
τ	PIN diode carrier lifetime	10.	μsec

active cells in each finger. Note that the quarter cells at edge of the fingers are inactivated by the P-well termination, so the number of active quarter cells is

$$N = (2a-2)(2b-2)c \tag{4.3}$$

as indicated in Fig. 4.4. Subtracting two from $2a$ and $2b$ effectively reduces the active cells at the end of every finger.

The device model is made by scaling up the cell model. Two area factors are introduced so that the effective areas can be optimized to compensate for the edge effect. Since N is used to scale up the currents as well as the charges from a quarter cell to a whole device, the extra area at the edge of the fingers results in a discrepancy in the gate charge calculation for small devices with a large edge effect. Thus, the factor f_{qga} is multiplied to the gate charge to reduce the discrepency. Note that f_{qga} is close to 1 for 700 cells or larger devices. Also, the junction charge is calculated with effective the area of both the bottom and the sidewall of the junction. The factor f_{qja} is multiplied by the junction charge calculation to account for the corner effect at the bottom and the sidewall of the junction. The factor f_{qga} and f_{qja} are extracted from gate capacitance vs. gate voltage and junction capacitance vs. drain voltage curve, respectively. Two extra parameters are taken from the SPICE channel model:f_{ns} is the subthreshold current fitting parameter that controls the subthreshold characteristics and f_{sh}, the short channel effect factor, is used to adjust the channel saturation voltage.

The other two empirical factors introduced are, f_{neff}, and f_{vth}. As discussed in the previous chapter, Region A limits current due to the effect of the

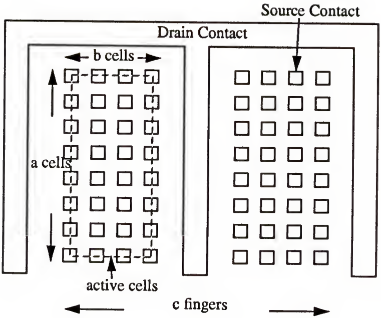


Figure 4.4 Simple layout schematic of a VDMOST, where the numbers of active quarter cells are *(2a-2)(2b-2)c.*

electron velocity saturation which brings up the electron concentration level (with a factor f_{neff} that links the electron concentration in high current and low current level) known as current-induce-space-charge. The factor obviously can be extracted from the I_D-V_{DS} curve at high V_{GS} (the quasi-saturation curve), but the high power curve is usually not seen. An alternative method to extract the parameter is from the I_D-V_{GS} curve. Since f_{neff} controls the special bending of the curve. The current level at the bending portion is used to determine f_{neff}.

The movement of the threshold voltage due to temperature difference is indicated by f_{vth}. Increasing the device temperature causes the decrease of the threshold voltage and the electron mobility. The factor f_{vth} defines the variation in the threshold voltages over the temperature range of interest as described in the next section.

Note that μ_{n00} and μ_{nd0} are process-dependent physical parameters and can be extracted by the process simulator or by checking the literature. The fitting parameter for the mobility θ can be obtained by fitting I_D-V_{GS} curve, as can be the threshold voltage V_{TH0}. The inversion threshold voltage in the epi region V_{THN} can be extracted by fitting the gate capacitance vs. gate voltage curves. R_{d0}, the drain contact resistance, has more effect during the turn-on of the PIN diode, so it can be extracted from the I_D-V_{DS} curves in reverse-mode operation along with f_m and f_{RS0}. The high injection carrier lifetime τ and transit time T_M inside the parasitic PIN diode are obtained from transient characteristics. The detailed parameter extraction routine will be discussed in Section 4.2 and 4.3.

4.2 Parameter Extraction Routine

With the device model installed in circuit simulators like SPICE or Saber, the model parameters regarding the steady-static characteristics and the capacitances can be extracted and optimized via ICCAP[ICC91]. In this case, ICCAP is used to interface the Saber simulator.

The measurement and the simulation system is shown in Fig 4.5. With the system, ICCAP is able to simulate using the VDMOST model in Saber. To link Saber with ICCAP, the Saber simulator must be indicated in the ICCAP simulator table and also selected in the main menu. The measurement equipment includes a HP4142, a modular dc source/monitor, for current-voltage measurements and a HP4284, a precision LCR meter, for capacitance-voltage measurements. High DC current measurement is required for power devices, but is difficult since the DC measurement equipment usually measure current up to only 100mA. A HP4142 measures current up to 1A, or 10A if a high current unit is installed. Both the units need the ground unit to sink the current, unlike regular 100mA units. The DUT probe station must be temperature controlled.

The three categories to be set up in ICCAP for the device model are the circuit deck, the parameter set and the DUT SETUP. The circuit deck defines the circuit network containing the DUT (device under test) at which the measurement is done. Here is defined the VDMOST model with the device entry, the node name and the default parameter values, which have exactly the same format as a Saber input deck. A set of model parameters is automatically generated with the default value. It can be altered through the parameter set menu as well.

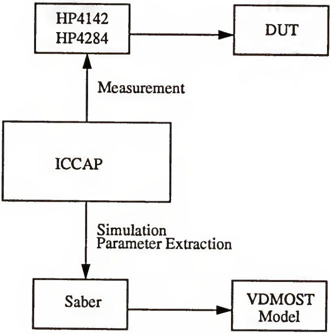


Figure 4.5 ICCAP/Saber system for measurement and simulation.

After parameter extraction or optimization is done, the table is renewed with the most recent values.

The DUT SETUPs specify the measuring and simulation conditions. Each SETUP also defines the parameters to be extracted from the measurement data. ICCAP comes with a variety of built-in model extractions that are described in the manual. The VDMOST model has a different parameter set, measurement requirements, and DUT SETUPs. Parameters must be extracted from the most relevant measurements. The sequence to perform the extraction for each SETUP is essential to obtaining good parameters, because the extraction depends on initial values of the parameters. The seven SETUPs for the VDMOST model is shown in Table 4.3. Each SETUP indicates a measurement and the parameters to be obtained from the measurement. By clicking on measurement for each SETUP, ICCAP performs the measurement. With the measurement data, the parameters are ready to be obtained either through extraction or optimization.

Parameter extraction is made through a user-defined procedure that calculates certain parameters from the measurement data by using physical equations. Optimization in ICCAP is the process of creating an optimum set of model parameter values. This optimum parameter set is created by adjusting the initial model parameter values in a iterative process. The process continues until simulated output data matches the actual measured data within specific tolerances.

The first SETUP idvd_r is the reverse mode $I_D - V_{DS}$ measurement. In this SETUP, the gate voltage is shorted to the source and the drain voltage is swept from 0V to -2V. The parameters of the parasitic PIN diode f_m, I_{RSO}, and

Table 4.3: ICCAP SETUPs for the parameter extraction.

SETUP	Description	Parameters obtained
idvd_r	Reverse mode $I_D - V_{DS}$ curve	f_m, I_{RS0}, R_{d0}
idvg	$I_D - V_{GS}$ curve at $V_D = 0.1V$	$\mu_{n00}, \mu_{nd0}, f_{ns}$, $V_{TH0}, \theta, f_{neff}$
idvd	$I_D - V_{DS}$ curve at $V_{GS} = 2 - 5V$	v_{sat0}, W, f_{sh},
cd_gs	$C_{DS} - V_{DS}$ curve with gate/source short	f_{qja}
cg_sd	$C_{GS} - V_{GS}$ curve with source/drain short	V_{THN}, f_{qga}
temp70	$I_D - V_{GS}$ curve at $V_D = 0.1V$ and $T = 70°C$	f_{vth} (1)
temp120	$I_D - V_{GS}$ curve at $V_D = 0.1V$ and $T = 120°C$	f_{vth} (2)

the series resistance in the buried layer R_{d0} are set to be extracted. The series resistance in the buried layer is important in both the forward and the reverse mode operation. It can be 30% of the on-resistance in the forward operation and almost all for the reverse operation. The on-state of the reverse $I_D - V_{DS}$ characteristics is almost linear with the reverse slope yielding the series resistance. The diode itself has very low on-resistance compared with this series resistance. The measurement and the simulated data for this SETUP is shown in Fig. 4.6.

The second SETUP idvg is the $I_D - V_{GS}$ measurement. In this SETUP, the drain voltage is 0.1V and the gate voltage is swept from 0V to 5V. This measurement reveals the on-resistance as a function of the gate voltage, the threshold voltage, the bending of the current due to large gate voltage, and also the subthreshold characteristics. As in conventional MOSFET models, this measurement is used to extract the threshold voltage V_{TH0}. For a VDMOST, the threshold voltage is not easy to define since the $I_D - V_{GS}$ curve doesn't have a constant slope when the gate voltage is higher than the threshold voltage. Instead, the curve has a peak slope between the threshold voltage and the current bending voltage. The threshold voltage is defined as the offset voltage of the tangent line at the peak slope of the $I_D - V_{GS}$ curve, as illustrated in Fig. 4.7. The on-resistance depends heavily on the electron mobilities, μ_{n00} and μ_{nd0} in this case, and it controls the slope of the $I_D - V_{GS}$ curve, so they can be obtained by this curve. The transverse-field fitting parameter θ controls the bending feature and the effective electron concentration fitting parameter f_{neff} controls the current level at the bending of the $I_D - V_{GS}$ curve, so are also obtained in the

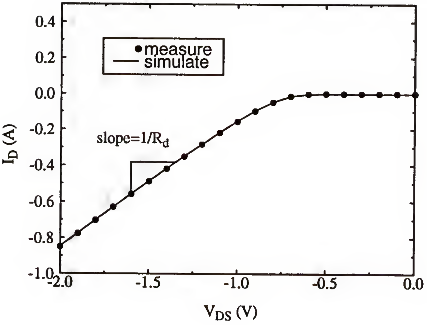


Figure 4.6 The simulated reverse-mode $I_D - V_{DS}$ curve compared with the measurement in idvd_r SETUP.

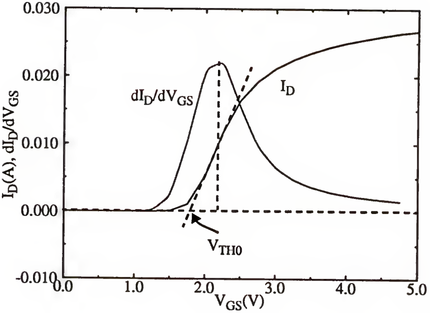


Figure 4.7 The extraction of the threshold voltage V_{THO}.

measurement. The subthreshold characteristics fitting parameter f_{ns}, has the effect on the curve below the threshold voltage. Fig. 4.8 shows the measurement with the simulation in this SETUP.

The other DC measurement done is the $I_D - V_{DS}$ curve in forward operation. In this measurement, the drain voltage is swept from 0V to 10V and the gate voltage is swept from 2V to 5V. This measurement which shows the saturation characteristics is used to extract the parameters related with the saturation characteristics. The electron saturated velocity is related to the saturation voltage. The effective channel width W controls the saturation current level and initially is two times the quarter cell window length except for the edge effect at the corner of the cell window. The short channel effect parameter f_{sh} in the level-0 channel model has a strong effect on the saturation voltage and the nearly-saturated current, so it is obtained in this measurement, too. The simulation result compared with the measurement is shown in Fig. 4.9.

The SETUPs cd_gs and cg_sd are the capacitance-voltage measurements. The former is the measurement of the drain/source capacitance vs. drain/source voltage with the gate shorted to the source and the drain voltage swept from zero to 10V. With the gate shorted to the source, the drain/source capacitance is almost the P/N junction capacitance because the gate/drain capacitance is much lower. As described in the previous section, the effective area of the gate charge is the product of the P-body area and the gate charge fitting parameter f_{qja}, which accounts for the corner effect at the junction bottom and side-wall. The parameter controls the junction charge (or drain/source capacitance) level, so the value

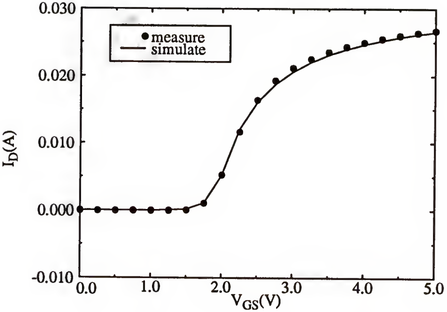


Figure 4.8 The simulated $I_D - V_{GS}$ curve compared with the measurement in idvg SETUP.

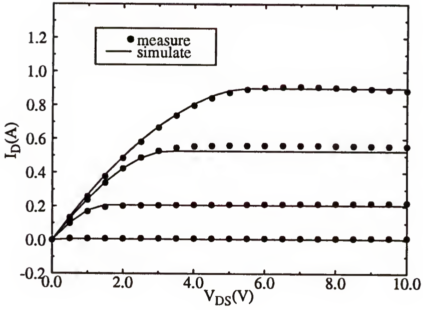


Figure 4.9 The simulated $I_D - V_{DS}$ curve compared with the measurement in idvd SETUP.

is optimized when the simulated drain/source capacitance has the best fit with the measurement data. The measurement and the simulated result of the drain/source capacitance is shown in Fig. 4.10.

The SETUP cg_sd is for the measurement of the gate capacitance vs. gate voltage with the drain shorted to the source and the gate voltage swept from -4V to 4V. This covers the accumulation, inversion, and depletion operation for the area under the gate. The measurement shows a dip between the threshold voltage and the epi-region inversion voltage. Since the edge of the fingers affects the effective area of the gate charge, the fitting parameter f_{qga} is introduced to even up the gate capacitance, and is obtained by the maximum capacitance (the flat portion) of the measurement over the oxide capacitance times NA_T. V_{THN}, the epi region inversion voltage, defines the voltage at the left side of the dip and can be observed from the curve. Figure 4.11 shows the measurement and the simulated curve of this SETUP.

The threshold voltage factor for the thermal effect f_{vth} is obtained from the variation of the threshold voltage over the different temperatures. In this case, all other parameters are obtained from the measurement done at the room temperature $20°C$ (nominal temperature). The $I_D - V_{GS}$ measurement at $70°C$ and $120°C$ in SETUPs temp70 and temp120 are done to obtain the threshold voltages. Two values of f_{vth} can be obtained from the $20°C/70°C$ and the $20°C/120°C$ measurements. Then, f_{vth} is defined as the average of the two values to ensure a more accurate value. Note that one SETUP that measures $I_D - V_{GS}$ at three different temperatures (sweeps the temperature parameter) can be used to

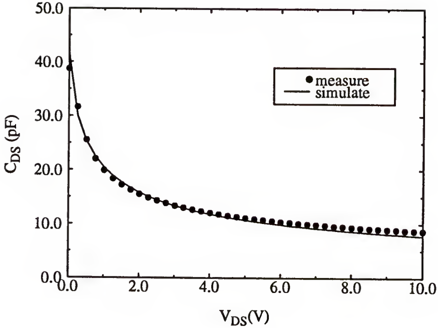


Figure 4.10 Simulated $C_{DS} - V_{DS}$ curve compared with measurement data in cd_gs SETUP.

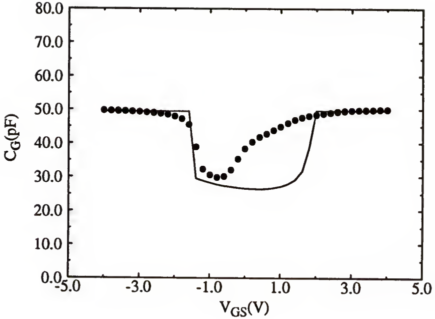


Figure 4.11 Simulated $C_G - V_{GS}$ curve compared with the measurement result in cg_sd SETUP.

replace the SETUPs temp70 and temp120 if the temperature control equipment can be linked to the ICCAP system. Figure 4.12 shows the $I_D - V_{GS}$ curves at $20°C$, $70°C$, and $120°C$.

4.3 Transient Parameter Extraction

The previous section regards the parameters taken from the steady-state characteristics and the capacitance-voltage characteristics. The other two parameters that are extracted from the transient characteristics are τ and T_M of the parasitic PIN diode. Following determination of the carrier lifetime from the reverse-recovery waveform in [TIE88], τ can be determined by

$$I_{RM} = a(\tau - \tau_{rr})\left(1 - exp\frac{T_1}{\tau}\right) \tag{4.4}$$

where I_{RM}, the peak reverse recovery current, and T_1, the peak reverse recovery time, are indicated in Fig. 3.13. a and τ_{rr} are constants obtained from the waveform directly with

$$a = -di/dt \text{ for } t \leq T_1 \tag{4.5}$$

$$i(t) = -I_{RM} exp - \frac{t - T_1}{\tau_{rr}} \text{ for } t \geq T_1 \tag{4.6}$$

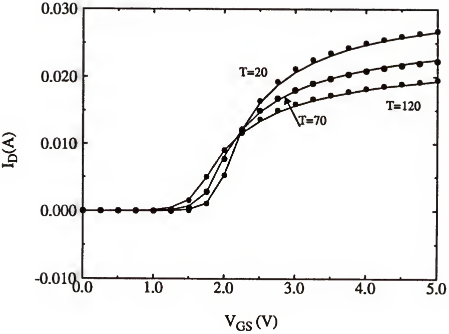


Figure 4.12 Simulated and measured $I_D - V_{GS}$ curves at temperature $20°C$, $70°C$, and $120°C$.

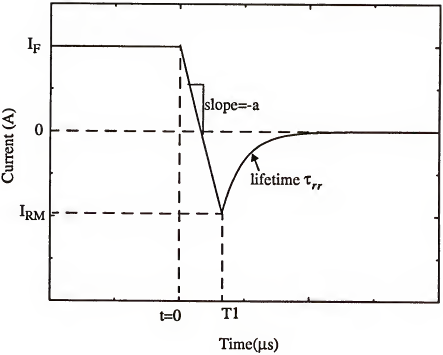


Figure 4.13 Reverse recovery waveform.

T_M then can be calculated from τ and τ_{rr},

$$1/\tau_{rr} = 1/\tau + 1/T_M \tag{4.7}$$

4.4 Circuit Simulation Examples

A physical circuit model not only has to be evaluated with the steady-state output characteristics and the capacitance-voltage characteristics as the traditional circuit simulator models, but it also has to pass the dynamic evaluations as well. According to the NIST working group [NIS94], typical model validation test procedures are expected to consist of test circuits that resemble application conditions, but that are simplified.

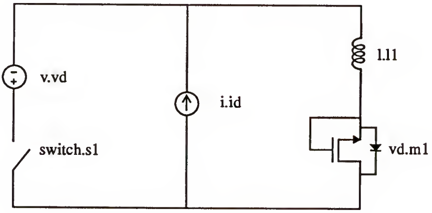
This section demonstrates the simulation of some of the test circuits with the VDMOST Saber template, including the reverse-recovery test circuit, the resistive-inductive loaded VDMOST, the zero-voltage switching circuit, and the gate-charge test circuit.

The reverse-recovery characteristics of a PIN diode taken from the response of an inductive load circuit. Fig. 4.14 shows the circuit with the VDMOST parasitic diode replacing the PIN diode by shorting the gate and the source. For the initial condition, the switch *switch.s1* is opened and the diode is in the forward state due to the current driving of the inductor *l.l1*. The switch is closed at 20 μsec; the discharge of the carriers in the N-epi region causes the current overshooting. Fig. 4.15 shows the simulated reverse-recovery character-

```
# Reverse Recovery Test Circuit

v.vd          d 1     =dc=-20
switch.s1     1 0     =sequence=(timed=[(0,o),(20u,c)])
i.id          0 d     =1
l.l1          d p     =70u
vd.m1         p p 0=n=2000, model= (tox=60n, LL=1.51u, Wt=5u,
              Nd=4.5e21,  Na0=1e23, As=12.4p, At=43.4p, Lov=300n,
              fm=2, irs0=10.56p, Rd0=1.319, vsat0=92.14k, un00=133.7m,
              und0=105.1m, W=4.816u, fsh=1e-21, fns=6.139, vth0=1.837,
              theta=6e-23, fneff=202.6m, fqja=1.593, vthn=-1.5, fqga=1.13,
              fvth=3.186m)
```

(a)



(b)

Figure 4.14 Circuit for testing the reverse-recovery current of the parasitic diode: (a) Saber input file and (b) circuit schematic.

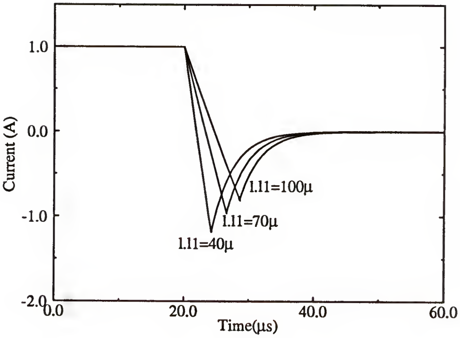


Figure 4.15 Turning-off of the parasitic diode showing the reverse-recovery current.

istics with different inductances.

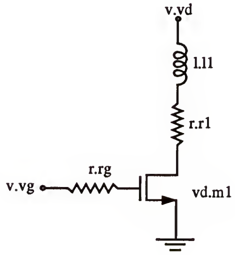
The inductive-load application is typical for power MOSFET. The simple circuit in Fig. 4.16 predicts how device capacitances influence switching with an inductive load. The VDMOST gate is driven from a voltage source with output impedance represented by *r.rg*. Fig. 4.17 shows the simulated transient turn-on and turn-off characteristics of the circuit. As the inductively-loaded MOSFET described in [WIL92], at the device turn-on, the gate voltage rises. The drain current starts to flow when the voltage is higher than the threshold voltage. When the drain current reaches the load current level (the inductor *l.l1* holds the current level), the drain voltage will fall from *v.vd* to the low ON-state voltage. This decreasing drain voltage produces a feedback current via the gate/drain capacitance to the gate, which must be provided by the gate drive. This feedback mechanism is the Miller effect that causes the increase of the effective gate/drain capacitance. Meanwhile, the gate voltage remains constant. Once the drain voltage falls to the low ON-state voltage, the gate voltage will increase toward the input voltage to maintain the current level.

At the turn-off of the device, the gate voltage falls off first. Then, the drain voltage rises while the drain current is almost fixed to the load current level. The gate voltage remains constant. The gate current charges the Miller capacitance at this phase. When the drain voltage reaches *v.vd*, the drain current turns off simultaneously with the decrease in the gate voltage.

It is well known in the power MOSFET that the nonlinearity of the gate capacitance make the gate circuit design difficult [GRA89]. The total gate

```
# Inductive-Resistive Load Test Circuit
vd.m1 0 g d =n=10000,model=(Rd0=0.0001)
r.rl        1 d        =30
r.rg        gg g       =2k
l.l1        dd 1       =2u
v.vg        gg 0       =tran=(pulse=(0,20,1u,20n,20n,29u,60u))
v.vd        dd 0       =dc=300
```

(a)



(b)

Figure 4.16 Circuit for transient simulations of a resistive-inductive load VDMOST: (a) Saber input file and (b) circuit schematic.

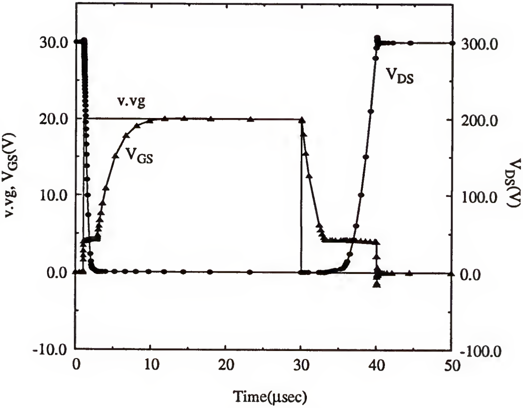


Figure 4.17 Saber simulated result of the resistive-inductive load VDMOST.

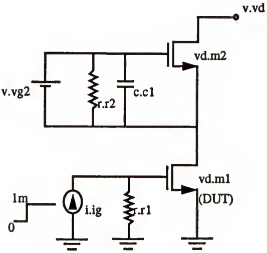
charge is specified that has to be supplied in order to establish a particular drain current under given test conditions. It permits a simple design methodology for obtaining any desired switching time, and it enables the total charge and the total energy required to be estimated easily. A schematic representation of the test circuit is given in Fig. 4.18. The use of constant-current sources for the supplies to the gate and drain greatly simplifies the turn-on transition.

Two VDMOSTs are used in this circuit: *vd.m1* is the device-under-test (DUT) and *vd.m2* is used as a current limiter that controls the maximum current of DUT. Initially, the DUT is OFF with the full line voltage applied across drain and source. At time zero, the gate current is switched into the device. With the gate current constant, the gate capacitances are charged at a constant rate. When V_{GS} reaches the threshold voltage, the DUT enters its active region and its drain current starts to rise. The rise of V_{GS} is unaffected and continues until reaching the current value set by the control MOSFET. At this point the drain voltage of the device-under-test starts of fall. The constant gate current discharges the Miller capacitance. Once the drain voltage has fallen to its ON-state value, the gate voltage resumes its constant upward rise for as long as the gate current continues. The rate of rise is lower than it was at first because of the higher value of the Miller capacitance. Fig. 4.19 shows the simulated gate-charge plot with the effect of an initial V_{DS} voltage.

Fig. 4.20 is another example of the VDMOST circuit simulations. The soft-switching circuit reduces switching losses provided in [KUR92] with a VDMOST as the device-under-test. It allows zero-voltage turn-on for the device

```
# Gate Charge test circuit
vd.m1      0  g  d =n=10000,model=(Rd0=0.0001)
r.r1       g    0  =10meg
i.ig       0    g   =tran=(pulse=(0,1m,0,1n,1n,60u,70u))
vd.m2      d  g2  dd =n=10000,model=(Rd0=0.0001)
v.vd       dd  0   =dc=100
c.c1       g2  d   =0.3u
r.r2       g2  d   =50k
v.vg2      g2  d   =dc=5
```

(a)



(b)

Figure 4.18 Gate charge test circuit: (a) Saber input file and (b) circuit schematic, note that the resistor r.r1 is required for the dc simulation, because there is no dc source at the gate of the VDMOST model:

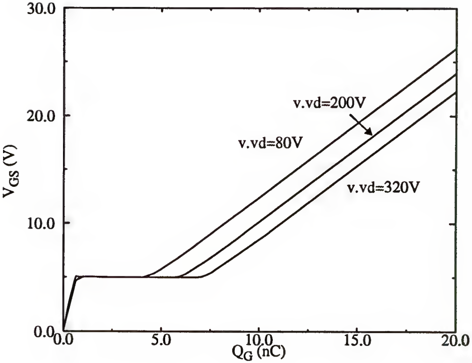
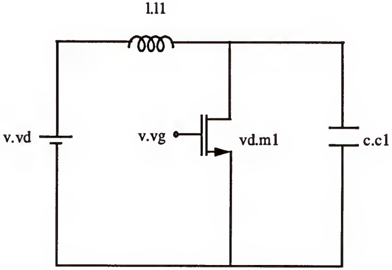


Figure 4.19 Total gate-charge vs. gate-to-source voltage with effect of initial drain-source voltage.

```
vd.m1 0 g d =n=100000
c.c1        d 0      =4u
l.l1        d 1      =15u
v.vg        g 0      =tran=(pulse=(0,12,2u,20n,20n,26u,80u))
v.vd        1 0      =dc=50
```

(a)



(b)

Figure 4.20 Soft switching circuit for transient simulations: (a) Saber input file and (b) circuit schematic.

under test, as in the simulation result shown in Fig. 4.21.

The parasitic BJT effect is shown in Fig. 4.22. With the gate shorted to the source, the drain is biased by a periodic pulse from 0 to 20V with 1 nano second rise time, fall time, and pulse width. The rapid increase of the drain voltage induces a displacement current across the pinch resistance R_P. The voltage drop can activate the parasitic BJT. The pinch resistance R_P ($\rho l/A$) is at the order of kilo ohm in a quarter cell. The simulation result shows V_{PS}, the voltage drop across R_P, and the parasitic BJT current I_{CT} with R_P=1KΩ, 2KΩ, and 3KΩ. The BJT has significant transient current when the base-emitter bias (V_{PS}) is higher than 0.5V.

4.5 Summary

In this Chapter, the VDMOST model implementation into Saber and SPICE2G6 are described. Structural as well as model parameters are stated in detail. Also, a system integrating ICCAP/Saber and measurement equipments is setup to obtain the model parameters. The SETUP in ICCAP permits automatic measurement, simulation and parameter extraction. The simulated steady-state characteristics and the capacitance-voltage characteristics are shown to have good agreement with the measurement data. Also, the transient simulations of circuits using the VDMOST template are demonstrated with the reverse-recovery test circuit, the resistive-inductive loaded VDMOST, the zero-voltage switching circuit, and the gate-charge test circuit suggested by NIST.

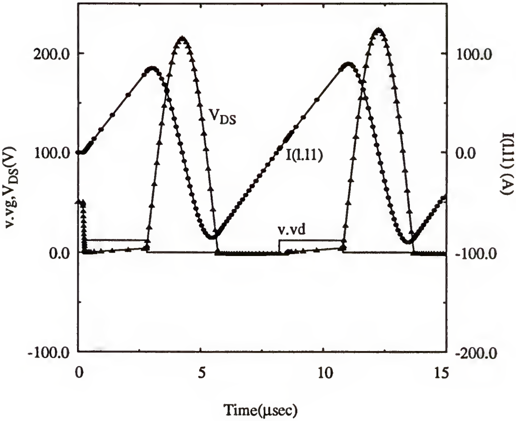
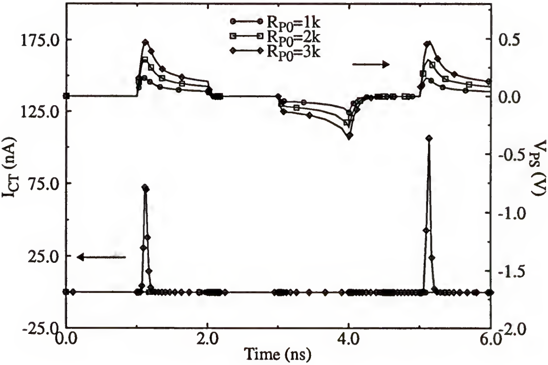


Figure 4.21 Saber simulated result for soft switching circuit.

```
vd.m1   0 g d     =n=1,model=(Rp0=2k)
v.vg    g 0       =dc=0
v.vd    d 0       =tran=(pulse=(0,20,1n,1n,1n,1n,4n))
```

(a)



(b)

Figure 4.22 (a) Saber input file and (b) simulated transient characteristics showing the parasitic BJT effect inside a VDMOST quarter cell. The drain is biased by a pulse from 0 to 20V with 1ns rise time and fall time. The displacement current in the P/N junction activates the parasitic BJT.

CHAPTER 5
SUMMARY AND SUGGESTIONS FOR FUTURE WORK

In this dissertation, a systematic approach for the physical modeling of semiconductor power devices is described and a model for the power VDMOST is developed and verified. Basic regional models provide a well-defined systematic approach for constructing circuit models and are driven by numerical simulations. By linking the regional models, a physical circuit model for a power device can be obtained that accounts for the unique behavior of the power device. A power VDMOST is used as an example for the systematic approach. Regions inside the VDMOST are defined according to extensive 2-D as well as 3-D device simulations. The composite model is implemented in Saber and SPICE2G6. The model accurately predicts quasi-saturation caused by the space-charge-limited current flow, reverse-recovery current of the parasitic PIN diode, nonlinear interelectrode capacitances in all operating regions, as well as on-resistance and saturation characteristics. Implementation of the temperature-dependent parameters to the model permits the difference of the operating temperature to the nominal temperature. Our new model is verified with test device measurements and numerical device simulations. A parameter extraction routine is developed and a system that links ICCAP and Saber is setup which integrates the measurement, the simulation, and the parameter extraction. Further circuit simulations of high-voltage ICs are done utilizing the Saber model template to demonstrate the excellent performance of our model for various applications.

Based on the research discussed herein, we suggest the following topics for future research.

First, we recommend a study of the optimum cell design of a VDMOST based on our modeling methodology. The on-resistance-area product is strongly dependent on the cell's geometric design and is predictable with our physical model.

Second, we recommend a investigation of the safe-operating-region for the VDMOST. The avalanche breakdown voltage for a cell depends on the drift-region doping, the device thickness, as well as the p-well spacing. The trade-off between the breakdown voltage and the on-resistance of a VDMOST is the most important design concern.

Third, we recommend the development of device-level model refinements. These might include better modeling of the distributed-effects in the actual multi-cell devices and the edge-effects at the sides of the active-regions that affect the currents, the gate capacitances, as well as the breakdown voltages.

Fourth, we recommend more indepth modeling of the thermal effect. For packaged power devices, the power generated in the chip interacts with the heat sink and the packaging, and modifies the operating temperature of the device. The robust Power IC CAD relies on the integration of the electrical and thermal systems.

APPENDIX A
BEHAVIORAL MODEL

A physical model is robust and predictive, but slow in CPU time because of the internal nodes and implicit equations. For a large circuit simulation, there is a need for a fast device model. Based on the simulated result of the physical model, a behavioral model for steady-state simulation is derived and implemented in Saber for the VDMOST. The behavioral model has little discrepancies and is much faster in simulation speed.

The behavioral model is based on a set of a I-V characteristics data simulated by the physical model. Instead of having internal nodes and physical equations, the drain current output is written as functions of external voltages V_{DS} and V_{GS} utilizing empirical equations. The parameters of the empirical equations are extracted by Kaleidagraph, a software with curve fitting ability.

It can be seen in the I_D-V_{DS} characteristics that the linear region current (I_{lin}), the saturation current (I_{sat}), and the saturation voltage (V_{sat}) are essential for the behavioral model. The goal is to represent them as functions of external voltages. I_{lin} is dependent on both V_{GS} and V_{DS}. According to its characteristics, I_{lin} is fit by

$$I_{lin} = \frac{aV_{DS}^{2} + bV_{DS}}{V_{DS} + c} \tag{1}$$

as shown in Fig.1, where a, b, and c, are the fitting parameters and are functions of V_{GS}. The three parameters a, b, and c versus V_{GS} are plotted in Fig. 2. and are fit by the sixth order polynomials of V_{GS} ($a,b,c=m_0+m_1V_{GS}^1+\sim+m_6V_{GS}^6$). The parameters $m_1 \sim m_6$ are shown in the graph, too. I_{sat} and V_{sat} are functions of V_{GS}, they are fit by

$$I_{sat} = \frac{m_1 V_{GS}^2 + m_2 V_{GS}}{V_{GS} + m_3} \tag{2}$$

and

$$V_{sat} = m_1 (V_{GS} + m_2)^{m_3} \tag{3}$$

Figure 3. (a) and (b) shows I_{sat} and V_{sat} in terms of V_{GS}. Thus the I-V characteristics can be constructed by the three variables, I_{lin}, V_{sat}, and I_{sat}

$$\text{if } V_{DS} < V_{sat} \text{ then } I_D = I_{lin} \text{ , else } I_D = I_{sat} \tag{4}$$

Figure 4 shows the similarity of the simulated I-V characteristics of both the behavioral model and the physical model. Saber execution time for the physical model is 196.7 seconds, and for the curve behavioral model is 35.8 seconds (5.5 times faster).

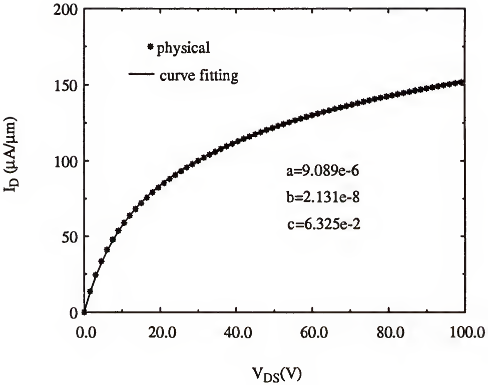
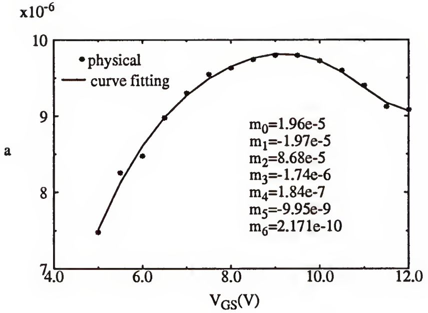
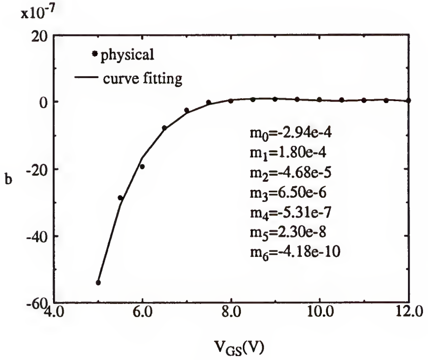


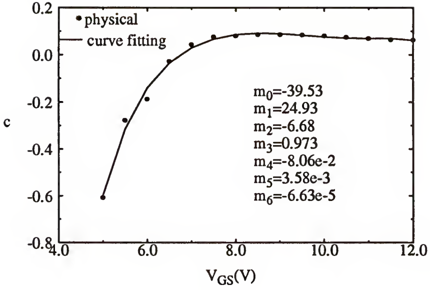
Figure 1 Drain current vs. drain/source voltage in the linear operating region (V_{GS}=12V). The drain current is fit by $y=(ax^2+bx)/(x+c)$, with x and y refer to the horizontal axis and the vertical axis, respectively.


x10^-6
10
9
8
7
a
• physical
— curve fitting
m0=1.96e-5
m1=-1.97e-5
m2=8.68e-5
m3=-1.74e-6
m4=1.84e-7
m5=-9.95e-9
m6=2.171e-10
4.0
6.0
8.0
10.0
12.0
VGS(V)

(a)

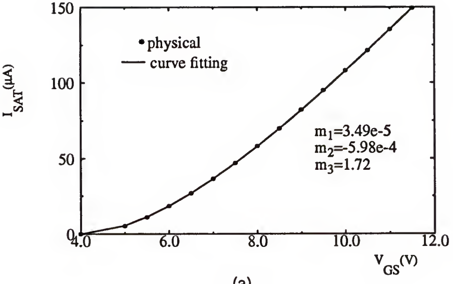

x10^-7
20
0
-20
-40
-60
b
• physical
— curve fitting
m0=-2.94e-4
m1=1.80e-4
m2=-4.68e-5
m3=6.50e-6
m4=-5.31e-7
m5=2.30e-8
m6=-4.18e-10
4.0
6.0
8.0
10.0
12.0
VGS(V)

(b)

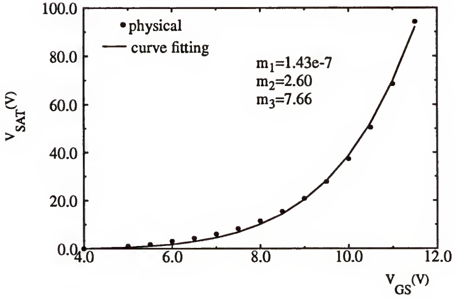


(C)

Figure 2 The parameters a, b, and c versus the gate/source voltage. They are fit by sixth order polynomial $y=m_0+m_1x+m_2x^2+m_3x^3+m_4x^4+m_5x^5+m_6x$.



(a)



(b)

Figure 3 (a) Saturation current versus gate/source voltage fit by $y=(m_1x^2+m_2x)/(x+m_3)$. (b) Saturation voltage versus gate/source voltage fit by $y=m_1*(x+m_2)^{m3}$.

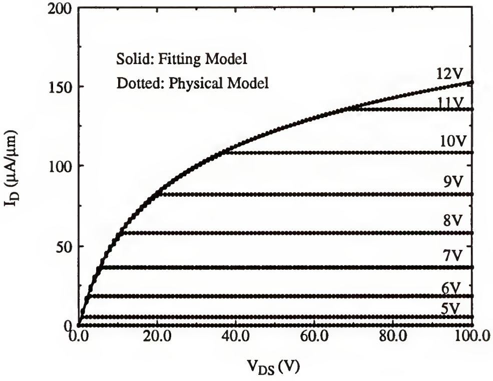


Figure 4 Simulated I-V characteristics of the VDMOST physical model(dotted) and the behavioral model(solid).

APPENDIX B
SABER TEMPLATE OF THE VDMOST MODEL

In this appendix, the saber implementation of the VDMOST model developed is listed. This model template includes regional models described in Section 3.1 with reverse-recovery body diode in Section 3.2 and the modification for the three dimensional structure in Section 3.3.

```
################################################################################
# This work was supported by the SRC under Contract # 92-SJ-285.
# Copyright, 1993, University of Florida.  All rights reserved.
# For further information, contact:
#                       Chin-yu Tsai  and  D.E. Burk
#                       address: tsai@tcad.ee.ufl.edu
#                       Oct. 4, 1993
################################################################################

# Physical quasi-3D VDMOST template
# all parameters are in M.K.S. unit

element template vd s g d =model,n,temp,tnom,ic

#Header declaration
electrical s,g,d

struc{
number  tox         =       1000.e-10,# oxide thickness
        Wt          =       20.u,   # epi region  depth
        Wj          =       6.4u,   # junction depth
        Na0         =       1.e23,  # channel doping peak
        Nd          =       1.1e21,# epi doping
        un00        =       0.13,   # channel region mobility
        und0        =       0.13,   # epi region mobility
        vsat00      =       1e5,    # channel saturation velocity
        vsatd0      =       1e5,    # drift region saturation velocity
        theta       =     0.,      # channel mobility trans. field. dep. coe.
        vthn        =     -4,      # drift inversion threshold voltage
        level       =     0,       # 0: Spice  1:Kim
        W           =     12.u,     # channel width
        LL          =     2.u,     # channel length
        fsh         =     0.3,     #short channel effect coefficient
        ns          =     3,       # subthreshold constant
        eta         =     2,       # channel doping gradient
        As          =     36.p,    # source contact area/quatercell
        At          =     225.p,   # gate-overlap area/quatercell
        Lov         =     0.3u,    # gate n+ overlapping length
        Rp0         =     100.,    # p body resistance (per u)
        vth0        =     2.7,     # gate threshold voltage
        fm          =     2.,      # reverse-mode diode current parameter
        Rd0         =     1,       # Burried layer resistance
        ibrs0       =     10u,     # Reverse bias diode saturation cur.
        tau         =     10u,     # PIN high injection lifetime
        tm          =     5u,      # PIN current transit time
        fneff       =     0.2,     # Neff coefficient
        fwdeff      =     0.,      # Wdeff coefficient
        fvth        =     0.009,   # threshold temperature coefficient
        fqja        =     1.5,     # Qj effective area factor
        fqga        =     1.1      # Qgd effective area factor
        }           model=()
number ic[2]=[undef,undef]
number n     =    200        # number of quatercells
number  temp        =     300      # device temperature
number  tnom        =     300      # nominal temperature
#Constants in MKS
{
number  icc0   =    1e-15            # parasitic BJT collector saturation current
number  ice0   =    1e-15            # parasitic BJT emitter saturation current
number  kpl         =     1.38e-23
number  que         =     1.6e-19
number  es          =     1.e-10
number  eso         =     3.45e-11
number  alpha       =     0.78
number  pi          =     3.14
number  Da          =     1e-3

#Values and variables declaration

number  phib,Cd0,Cox,vbi,Ec,icr1,phibn,vfbn,vfbp
number  Rp, di,lamb,BB,F,vm,Ap,Lp,Ls,Ldeb,ias
number  vt,un0,und,vsat0,vsatd,vth,mn,mp,Eg,Ni,ibrs,L,Rd
val     v          vds,vgs,va,vb,vc,vchp,vche,vch,vps,vpb,this,vr,thi,von
val     i           ich,ict,ibr,iid,iida,ip,ich0
val     q           Qn0,Qnl,Qj,Qgs,Qgd,Qp,Qsi,Qs,Qe
val     meter       Wc,Wdeff,Wa,Wb
val     nu          un,ux,consvb,neff,ac,bc,Aa,Kvb,Kvb2,Cd,bp,cp,kp,
                    mob1,mob2,Cdp,kvch,flag,flag1,acc,bcc
var     i           id,ida
var     meter       Wdep
var     q           Qm

group   {vds,vgs,vch,vpb,vps,va,vb,vc} v
group   {ich,iid,iida,ict,ibr} i
group   {Qj, Qgd, Qgs, Qp,Qsi}Q

electrical p,a,b,d1

struc   sa_point {numberbp,inc;}\
        sv[*]=[(-1meg,1k),(-500,50),(-
50,0.1m),(0,0.1m),(50,0.1),(1000,0.1meg),(1meg,0)],
        sid[*]=[(-1meg,1k),(-2m,10u),(0,0.001u),(100u,.1u),(1,0.1meg),(1meg,0)],
        sWdep[*]=[(0,1n),(20u,1u),(200u,0.1k),(1k,0)],
        svpb[*]=[(-100k,0.1),(-10,.001),(0,0.1),(10,1k),(1meg,0)],
        sthi[*]=[(-1e10,1k),(-100,1),(-1,1m),(0,1m),(1,1),(100,100),(10k,0)],
        nv[*]=[(0,0.1),(2,1k),(1meg,0)],
        svd[*]      =[(-300,1),(-10,.1),(-1.5,.1m),(0,.1),(3,1),(100,10),(1k,10)],
        sQm[*]  =[(-300,1),(-10,1n),(0,1n),(10u,1u),(1m,10m),(1,10),(1k,0)],
        nvd[*]      =[(-2,0.1),(0,.1),(1,0)]
#       sd[*]=[(0,1e2),(1e10,0)]

#-----------------------------------------
parameters {
vt      =kpl*temp/que
un0     =model->un00*(tnom/temp)**2.5
und     =model->und0*(tnom/temp)**2.5
vsat0   =model->vsat00*(tnom/temp)**0.87
vsatd   =model->vsatd0*(tnom/temp)**0.87
vth     =model->vth0-model->fvth*(temp-tnom)
mn      =1.034+5.826e-4*temp-2.826e-7*temp**2
mp      =0.552+1.1e-3*temp-7.769e-7*temp**2
Eg      =1.179-9.025e-5*temp-3.05e-7*temp**2
ni      =4.9e15*(mn*mp)**0.75*temp**1.5*exp(-Eg/2*Kpl/temp)
ibrs    =model->ibrs0*exp(-que/Kpl*Eg*(1/temp-1/tnom))
Rd      =model->Rd0**(temp/tnom)**1.5
L       =model->LL
Ls      =(model->As)**0.5
Cox     =eso/model->tox
phib    =vt*ln(model->Na0/Ni)
```

```
vbi      =vt*ln(model->Nd*model->Na0/Ni**2)
Cd0      =(que*es*model->Na0/(4*phib))**0.5
Ec       =vsatd/und
phibn  =vt*ln(model->Nd/Ni)
vfbn     =vth
Rp       =model->Rp0/n
Ap       =model->As*(1+(model->Lov+L)/Ls)**2
Lp       =Ls+model->Lov+L
ias      =(model->At-Ap)*que*model->Nd*vsatd
Ldeb     =(es*vt/que/model->Na0)**0.5

}
#---------------------------------------------
values {
vds      =v(d1)-v(s)
vgs      =v(g)-v(s)
vch      =v(a)-v(s)
vpb      =v(p)-v(b)
vps      =v(p)-v(s)
vr       =v(d1)-v(d)


# Physical parameters
un       =un0/(1+model->theta*(vgs-vth))
Qn0      =Cox*(vgs-vth)

################################################################
# active MOS region
################################################################

# Critical voltages, velocity saturates at either end
if (model->level==1) {
bp       =2*Cox*(vgs-vth)+2*model->eta*Cd0*phib
cp       =Cox+Cd0
kp       =model->W*n*un/2/L

# velocity saturate at drain end
vchp     =(Cox*(vgs-vth)+2*model->eta*Cd0*phib)/(Cox+Cd0+un*Cox*(vgs-vth)/
(2*L*vsat0))
Cdp      =Cd0*(1-2*model->eta*phib/(vchp+1e-10))
ip       =model->W*n*vsat0*Cox*(vgs-vth-vchp*(1+Cdp/Cox))
if (vgs<=vth) {
ich      =0
}

else     {
```

```
mob1=-(2*ip-kp*vchp*bp)/(vchp*ip+1e-10)
mob2=(-kp*vchp**2*cp+ip)/(vchp**2*ip+1e-10)

if (abs(vch)<vchp) {
          vche          =abs(vch)
          ux            =un/(1+mob1*vche+mob2*vche**2)
if (vch>0) {
ich=abs(model->W*n*ux/(2*L)*vche*(2*Cox*(vgs-vth)-(Cox+Cd0)*vche+2*mod-
eleta*Cd0*phib))
}
else      {
ich=-abs(model->W*n*ux/(2*L)*vche*(2*Cox*(vgs-vth)-(Cox+Cd0)*vche+2*model-
>eta*Cd0*phib))
}
}

          else {
          vche          =vchp
          ich           =abs(ip)*vch/abs(vch)
             }
Cd        =Cd0*(1-2*model->eta*phib/(vche+1e-10))
Qnl       =Cox*(vgs-vth-vche*(1+Cd/Cox))
}
}

else {
von=vth+model->ns*vt
if (vgs>von) {
 vchp=-vsat0*L/un+((vsat0*L/un)**2+2*vsat0*L*(vgs-vth)/un/(1+model->fsh))**0.5
}
else {
vchp=-vsat0*L/un+((vsat0*L/un)**2+2*vsat0*L*model->ns*vt/un/(1+model-
>fsh))**0.5
}

# Linear region current
if (abs(vch)>vchp) {
          vche=vchp
          }
else {
          vche=abs(vch)
          }
ich0=abs((n*un*Cox*model->W/L/(1+un*vche/vsat0/L)*vche*(model->ns*vt-
(1+model->fsh)*vche/2)))*abs(vch)/(vch+1e-10)
if (vgs>von) {
ich=abs((n*un*Cox*model->W/L/(1+un*vche/vsat0/L)*vche*(vgs-vth-(1+model-
>fsh)*vche/2)))*abs(vch)/(vch+1e-10)
}
        else {
        ich=ich0*exp((vgs-von)/model->ns/vt)
        }
}

######################################################################
# drift region
######################################################################

#********* region A
if (vch+va>0) {
        Wdeff           =Wdep
                        }
        else {
        Wdeff           =0
        }
        Aa              =model->At-Ap*(1+Wdeff/Lp*model->fwdeff)**2
        if (ida>0)      {
        if (ida>(1+model->fneff)*ias) {
        neff=ida/(Aa*que*vsatd)
        }
        else {
        neff=model->Nd+model->fneff*model->Nd*exp((ida/ias-(1+model->fneff))/
model->fneff)
                        }
va=ida*(model->Wj+Wdeff)/(Aa*que*neff*und)+que*(neff-model->Nd)*(model-
>Wj+Wdeff)**2/es/2
        }
        else            {
        va              =0
        }

# *********** B region
#       consvb=(1u*que*model->Nd*und*(Ld+Lp))/(1u*que*model->Nd*und*Ld)
#       vb              =id*tan(alpha)/(1u*que*model->Nd*und)*ln(abs(consvb+1e-40))

if (model->Wt>model->Wj+Wdep+Lp) {
        Wb              =Lp
        }
else    {
        Wb              =model->Wt-model->Wj-Wdep
        }
        kvb             =(abs(model->At-id/(2*que*model->Nd*und*Ec))/Ap)**0.5
        kvb2            =ln(abs((kvb+1-Wb/Lp)/(Kvb-1+Wb/Lp)))
```

```
vb=Lp/2/Ap*tan(alpha)*id/(que*model->Nd*und)/kvb*(ln(abs((kvb+1)/(Kvb-1)))-kvb2)
# ********** C region
        Wc              =model->Wt-model->Wj-Lp*tan(alpha)-Wdeff
        if (Wc>0) {
        vc              =id*Wc/(model->At*que*model->Nd*und-id/Ec)
        }
        else            {
        vc              =0
        }
        iid=id*n
        iida=ida*n

#************* Q
###### Qj
if (vpb<vbi) {
        Qj              =n*Ap*model->fqja*(2*que*es*model->Nd*abs(-vpb+vbi))**0.5
}
else {
        Qj              =0
# W*Lp*(2*que*es*model->Nd*abs(vbi))**0.5
}

###### Qgs

# Body charge Qsi
        # body accumulation
        if (vgs<vfbp) {
                        Qsi     =-Cox*(vgs-vfbp)*n*(Ap-(1+model->Lov/Ls)**2*model-
>As)
        }
        # body depletion
        else if(vgs<vth) {
        acc             =vgs-vfbp
        bcc             =2*que*es*model->Na0/Cox**2
        thi             =acc+bcc/2-abs(bcc**2/4+acc*bcc+1e-15)**0.5
Qsi=-abs(2*que*es*model->Na0*thi+1e-15)**0.5*n*(Ap-(1+model->Lov/
Ls)**2*model->As)
        }

        #body inversion
        else {
        acc             =vth-vfbp
        bcc             =2*que*es*model->Na0/Cox**2
        thi             =acc+bcc/2-abs(bcc**2/4+acc*bcc+1e-15)**0.5
Qsi=(-(2*que*es*model->Na0*thi)**0.5-Cox*(vgs-vth))*n*(Ap-(1+model->Lov/
Ls)**2*model->As)
```

```
        }

        Qgs         =(n*(model->As*(1+model->Lov/Ls)**2-model->As))*Cox*vgs-
Qsi/2
###### Qgd
# drift accumulation
if (vgs-vch>vfbn) {
         Qgd        =n*(model->At-Ap)*Cox*(vgs-vch-vfbn)-Qsi/2
        flag        =1
        }

# drift inversion
else if (vgs-vch<model->vthn & vch<vchp){
        ac          =model->vthn-vfbn
        bc          =(2*que*es*model->Nd)**0.5/Cox
        this        =abs(bc**2-2*ac-bc*(bc**2-4*ac)**0.5)/2
        Qgd         =n*(model->At-Ap)*Cox*(vgs-vch-model->vthn)-n*(model->At-
Ap)*bc*(this)**0.5*Cox-Qsi/2
        flag=3
        }
# drift depletion
else    {
        ac          =vgs-vch-vfbn
        bc          =(2*que*es*model->Nd)**0.5/Cox
        this        =abs(bc**2-2*ac-bc*(bc**2-4*ac+1e-15)**0.5)/2
        Qgd         =-n*(model->At-Ap)*bc*(this+1e-20)**0.5*Cox-Qsi/2
        flag=2
        }
ict     =icc0*n*limexp(vps/vt)-ice0*n*limexp(vpb/vt)


# ***********************************************
#       Reverse mode, PIN diode
# ***********************************************

#if     (vds<0) {
#ibr    =Ap*n*2*que*Da*Ni*F*(limexp(-vds/vt/model->fm)-1)/di
#ibr    =ibrs*n*(limexp(-vds/vt/model->fm)-1)
#Qp     =model->tou*ibr
Qe      =model->tau*model->ibrs0*(limexp(-vds/(vt*model->fm))-1)

#}
#else   {
#ibr    =0
#Qp     =0
#}
```

```
}
#--------------------------------------------
Control_section {
# initial conditions and start value
initial_condition(vgs,ic[1])
initial_condition(vds,ic[2])
sample_points(vch,sv)
sample_points(vpb,svpb)
sample_points(vps,svpb)
sample_points(id,sid)
sample_points(ida,sid)
sample_points(Wdep,sWdep)
sample_points(vds,svd)
sample_points(Qm,sQm)
newton_step(vds,nvd)
}
#--------------------------------------------

equations {

i(g->s)             +=d_by_dt(Qgs*model->fqga)
i(g->a)             +=d_by_dt(Qgd*model->fqga)
i(d1->b)            +=id*n
i(b->a)             +=ida*n
i(a->s)             +=ich
i(b->s)             +=ict
i(b->p)             +=d_by_dt(Qj)
i(p->s)             +=vps/Rp
i(d1->d)            +=vr/Rd
id:      v(d1)-v(b)=vb+vc
ida:     v(b)-v(a)=va
Wdep:    Wdep=abs(2*es*abs(vch+va)/(que*model->Nd)+1e-40)**0.5
i(s->d1) +=n*(Qe-Qm)/model->tm
Qm:      0=d_by_dt(Qm)+Qm/model->tau-(Qe-Qm)/model->tm
}
}
```

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